SAM3308B

Multi-purpose Audio DSP

Real-time audio applications in professional quality…

- Wavetable synthesis
- MP3 decoding
- Effect processing (reverb, echo, chorus, equalizer …)
- Filtering, sampling rate conversion

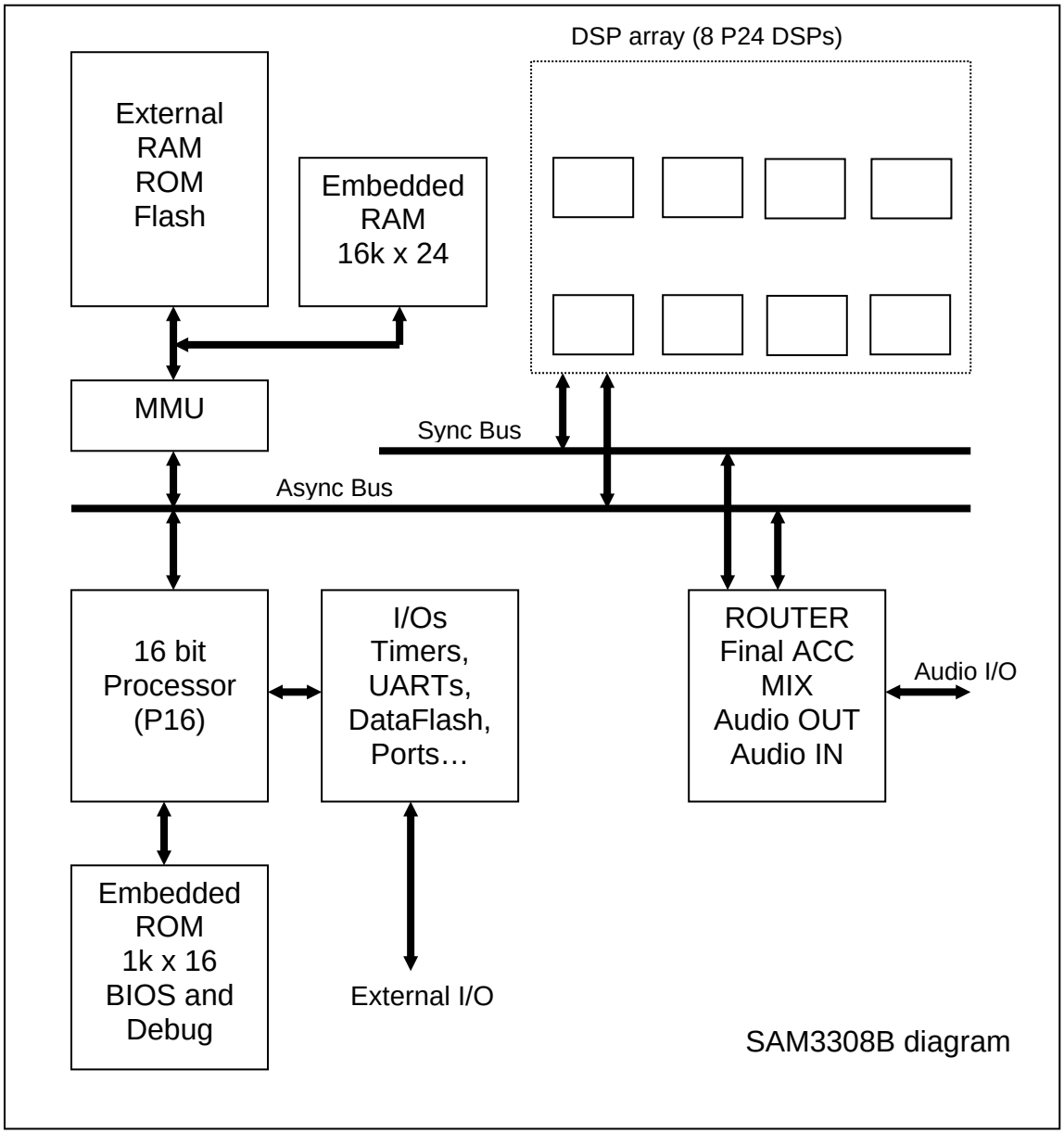
for audio products…

- Karaoke
- Professional audio
- Cellular phones
- Musical instruments
- Consumer electronic

at the best performance / price.

- 8 DSPs and Audio Router on chip (24 bit)
- 32kHz to 96kHz sampling rate
- Microcontroller on chip (16 bit)
- Variety of I/O, including SmartMedia™ and DataFlash®
- Embedded RAM for single chip operation (768 Kbit)
- Warm start power-down
- 1µA typ. deep power down, 0.5mW / Mips typ. operating
- LQFP100, external Flash/ROM capability

1. Dream DSP Array™ Overview



- DSP Array

The SAM3308B includes 8 DSPs on chip.
Each DSP (P24) is built around a 2k x 24 RAM and a 1k x 24 ROM. The RAM contains both data and P24 instructions, the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.
Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop.
One P24 is sufficient for processing one channel of MP3 data pump, implementing a multitap delay line or a multi-tap transversal filter. A single P24 is also capable of generating 12 voices of wavetable sound at 32KHz sampling rate (8 voices at 48KHz), including sample cache, pitch control, 2nd order filter and two envelope generators.

- Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 64 time slots. Each slot is divided into 4 bus cycles. Each P24 is assigned a hardwired time slot (8 to 63), during which it may provide 24 bit data to the bus (up to 4 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 7 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

- Async Bus

The Async Bus is 24 bit data inside the chip and 16 bit outside.
The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external or embedded ROM/RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

- 16-bit processor

This is the P16 processor, widely used in Dream products. Using the P16 allows to keep the large firmware investments from the SAM97xx series. A built-in ROM, connected to the P16 holds basic input/output software (BIOS) for peripherals such as UART, DataFlash®, SmartMedia®, MPU, as well as a debugger which uses a dedicated asynchronous serial line. The firmware can reside on external parallel ROM/Flash or it can be downloaded at power-up into the built-in 16kx24 RAM from serial EEPROM, DataFlash, SmartMedia or host.

- MMU (memory management unit)

The MMU handles transfer requests between the external or embedded RAM/ROM, the P16 and the P24s through the Async Bus. The SAM3308B includes 16k x 24 RAM on chip.

- Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 8 channels of audio in and 8 channels of audio out are provided (4 stereo in/out, I2S format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

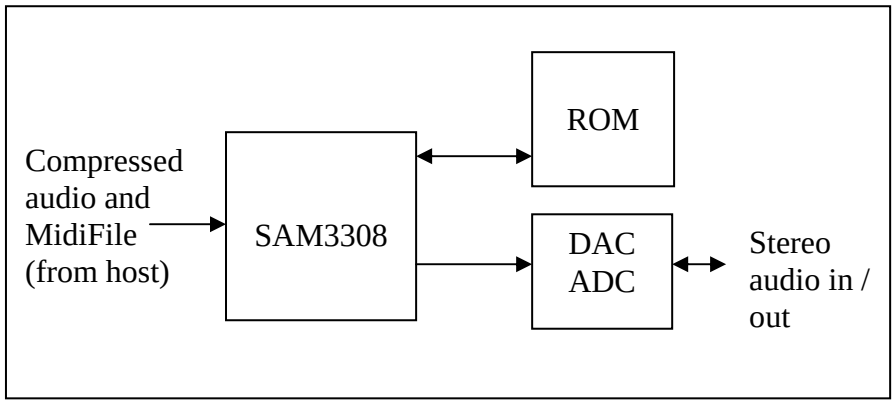
- I/O

The SAM3308B includes very versatile I/Os, which share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.
Following peripherals are included on chip:

- 2 x 8bit timers
- 2 x 16bit timers
- Parallel slave 8 bit port, MPU401 compatible
- Parallel master 8 bit port, for connection to SmartMedia and/or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial ports
- Synchronous serial slave port (SPI type host connection).
- SPI master bi-directional port for EEPROM or DataFlash connection.
- Firmware controlled I/O pins.

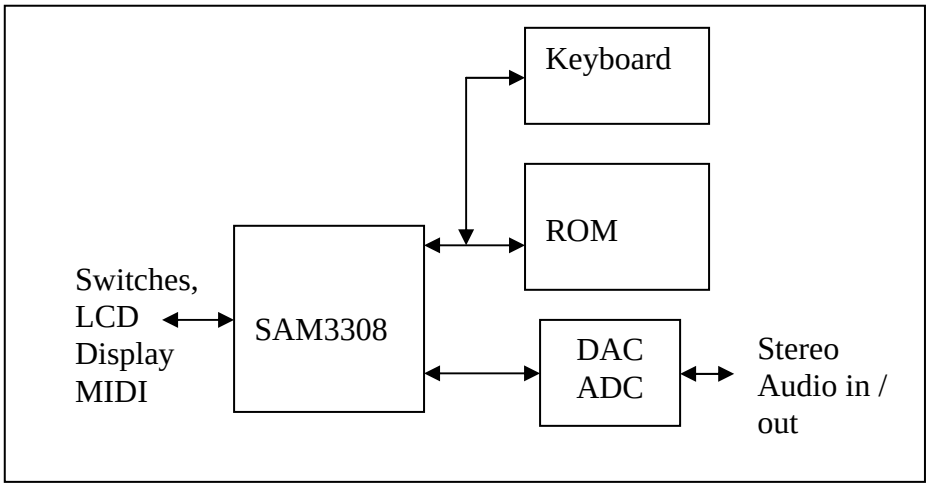
2. Typical application examples

2.1. Host controlled MP3 + high quality wavetable player



- Concurrent MP3 + wavetable
- Legendary Dream high quality wavetable sound
- Typical polyphony:
  - 56 voices with effects (reverb, chorus, …) @48kHz sampling rate
  - MP3 decode + 32 voices with effects @48kHz sampling rate
- External wavetable ROM/Flash choice from 4Mbit to 128Mbit
- Choice of host communication interfaces:
  - 8 bit parallel
  - Asynchronous serial (MIDI)
  - Synchronous serial (SPI)
- Built-in Standard Midi file player (SMF) dramatically reduces host load

2.2. Musical keyboard with key velocity



- Up to 64 voices polyphony with effects
- Choice of GM+ sampled sounds from 4Mbit to 64Mbit
- Maximum external memory addressing range: 128Mbit

3. DSP capacity and I/O configuration

3.1. DSP considerations

The SAM3308B includes 8 x P24 DSPs.
The table below lists the performance achievable by the P24:

Function	P24s required
MP3 decode	3
12 voice wavetable synthesis @32kHz	1
8 voice wavetable synthesis @48kHz	1
Stereo reverb and chorus @48kHz	1
Stereo 31 band equalizer @48kHz	3

The SAM3308B runs firmware directly from an external ROM/Flash memory. It may also run firmware from local RAM, thus freeing many I/O pins, which can then be used for application dependent functions. The SAM3308B is the ideal choice when wavetable synthesis or many I/O pins are required.

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pinout to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host controlled operation

There are 3 main possible ways of communication with a host processor:

- 8 bit parallel MPU type bi-directional interface
  signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial, MIDI_IN and optionally MIDI_OUT
- Synchronous serial
  signals: SDIN, SCLK, SYNC, INT/

3.2.2. Stand alone operation

Possible stand-alone modes are:

- Firmware into external ROM or Flash memory
- Firmware into external EEPROM or DataFlash
- Firmware into external SmartMedia. In this case, the firmware should reside in the SmartMedia reserved sectors starting at sector # 1.

4. Pinout

4.1. Pin description

Identical sharing number indicates multifunction pins.
Pd indicates pin with built-in pull-down resistor.
Pu indicates pin with built-in pull-up resistor.

Pin name	Pin#	Type	Sharing	Description
GND	9,22,30, 41,56,70, 75,87,97	PWR	-	Digital ground, all these pins should be returned to a ground plane
VC18	20,47,73, 99	PWR	-	Core power, all these pins should be returned to nominal 1.8V or to PWROUT if the built-in power switch is used.
VC33	13,50,83	PWR	-	Periphery power, all these pins should be returned to nominal 3.3V.
PWRIN	29	PWR	-	Power switch input, should be returned to nominal 1.8V even if the power switch is not used
PWROUT	28	PWR	-	Power switch output, should be connected to all VC18 pins if the power switch is used
D7-D0	96,95,91, 90,82,81, 77,76	I/O	1	Slave 8bit interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0 input.
I/O7-I/O0	96,95,91, 90,82,81, 77,76	I/O	1	SmartMedia data or other peripheral data
P0.7-P0.0	96,95,91, 90,82,81, 77,76	I/O	1	General purpose I/O can individually be programmed as input or output
CLAD3-0	96,95,91, 90	In	1	Optional bit clocks and word selects for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
WSAD3-0	82,81,77, 76	In	1	
A0	98	In	2	Slave 8bit interface address. Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low)
SMPD	98	In	2	SmartMedia presence detect
P0.10	98	In	2	General purpose input pin
SCLK	98	In	2	Serial slave synchronous interface input clock
CS/	100	In	3	Slave 8bit interface chip select, active low.
P0.11	100	In	3	General purpose input pin
SYNC	100	In	3	Serial slave synchronous interface input sync signal
WR/	1	In	4	Slave 8bit interface write, active low. D7-D0 data is sampled by chip on WR/ rising edge if CS/ is low
SMC/	1	In	4	SmartMedia configuration. This pin is sensed after power-up. If found low, it is assumed that a SmartMedia connector is present. The built-in firmware will wait for SmartMedia SMPD.
P0.12	1	In	4	General purpose input pin
RD/	2	In	5	Slave 8bit interface read, active low. D7-D0 data is output when RD/ goes low and CS/ is low
R|B/	2	In	5	SmartMedia Ready Busy/ status
P0.13	2	In	5	General purpose input pin
IRQ	8	Out	6	Slave 8bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0)
SMRE/	8	Out	6	SmartMedia read enable (RE/), active low
FS0	8	In	6	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
P0.8	8	I/O	6	General purpose I/O pin

INT/	8	Out	6	Serial slave synchronous interface data request, active low.
MIDI_IN	17	In	7	Serial MIDI in
P0.14	17	In	7	General purpose input bit
SDIN	17	In	7	Serial slave synchronous interface input data
MIDI_OUT	18	Out	8	Serial MIDI out
FS1	18	In	8	Freq sense, sensed at power up. FS1|FS0 allow firmware to know operating freq of chip as follows: 00- 6.9552 MHz 01- 9.6 MHz 10- 11.2896 MHz 11- 12.288 MHz
P0.9	18	I/O	8	General purpose I/O
DABD3-0	67,66,65, 64	Out	-	4 stereo channels of digital audio output, I2S format
CLBD	6	Out	-	Audio bit clock for DABD3-0. Audio bit clock for DAAD3-0 if the corresponding CLAD3-0 is not used.
WSBD	7	Out	-	Audio left/right channel select for DABD3-0. Audio left/right channel for DAAD3-0 if the corresponding WSAD3-0 is not used.
CKOUT	5	Out	-	External DAC/Codec master clock. Same frequency as X2 pin. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, Fs being the DAC/Codec sampling rate.
DAAD0	54	In	9	Stereo audio data input, I2S format. Can operate on CLBD master rate or CLAD0 external rate when sampling rate conversion is requested.
P0.15	54	In	9	General purpose input pin
DAAD3-1	60,59,55	In Pd	-	3 additional channels of stereo audio input, I2S format. Can individually operate on CLBD master rate or corresponding CLAD3-1 when sampling rate conversion is requested. DAAD3-1 have built-in pull-downs. They may be left open if not used.
MUTE	19	I/O	10	External DAC/Codec Mute. Sensed at power up. If found high then MUTE becomes an active high output. If found low, then MUTE becomes an active low output.
P1.6	19	I/O	10	General purpose I/O pin
WA21	45	Out	11	External memory address bit, extension to 64 Mbits
SMCE/	45	Out	11	SmartMedia chip enable (CE/), active low
P1.5	45	I/O	11	General purpose I/O pin. P1.5 cannot be used as output if DFCS/ pin is used. Indeed DFCS/ pin is internally driven by P1.5 GPIO.
WA20	44	Out	12	External memory address bit, extension to 32 Mbits
SMALE	44	Out	12	SmartMedia address latch enable (ALE)
P1.4	44	I/O	12	General purpose I/O pin
WA19	43	Out	13	External memory address bit, extension to 16 Mbits
SMWE/	43	Out	13	SmartMedia write enable (WE/), active low
P1.3	43	I/O	13	General purpose I/O pin
WA18	42	Out	14	External memory address bit, extension to 8 Mbits
SMCLE	42	Out	14	SmartMedia command latch enable (CLE)
P1.2	42	I/O	14	General purpose I/O pin
WA17 – WA16	58,57	Out	15	External memory address bits, extension to 2 and 4 Mbits
P1.1 – P1.0	58,57	I/O	15	General purpose I/O pins
WA15 – WA0	53,51,40, 39,38,37, 36,27,26, 21,16,15, 14,12,11, 10	Out	16	External memory address bits, up to 1 MBits (64k x 16)
P2.15 – P2.0	53,51,40, 39,38,37, 36,27,26, 21,16,15, 14,12,11, 10	I/O	16	General purpose I/O pins

WD15 – WD0	94,93,92, 89,88,86, 85,84,80, 79,78,69, 68,63,62, 61	I/O	17	External memory data
P3.15 – P3.0	94,93,92, 89,88,86, 85,84,80, 79,78,69, 68,63,62, 61	I/O	17	General purpose I/O pins
WCS1/	3	Out	18	External memory chip select 1, active low. Pre-decode for an external RAM/Flash/ROM at address 200:0000H.
P1.10	3	I/O	18	General purpose I/O pin
WCS0/	4	Out	19	External memory chip select 2, active low. Pre-decode for an external RAM/Flash/ROM at address 000:0000H
P1.9	4	I/O	19	General purpose I/O pin
WOE/	48	Out	20	External memory output enable, active low.
P1.8	48	I/O	20	General purpose I/O pin
WWE/	49	Out	21	External memory write enable, active low.
P1.7	49	I/O	21	General purpose I/O pin
DFCS/	23	Out	-	DataFlash chip select. When DFCS/ pin is used, P1.5 GPIO cannot be used as output. Indeed DFCS/ pin is internally driven by P1.5 GPIO.
DFSI	25	Out	-	DataFlash serial input (to DataFlash)
DFSO	32	In Pd	-	DataFlash serial output (from DataFlash). This pin has a built-in pull-down. It may be left open if not used.
DFSCK	24	Out	-	DataFlash data clock
P1.15	46	I/O Pu	-	General-purpose I/O pin. This pin has built-in pull-up. It may be left open if not used.
X1 – X2	72,71	-	-	External crystal connection. Standard frequencies are 6.9552 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. 1.8Vpp) can be connected to X1 using AC coupling (22pF). A built-in PLL multiplies the clock frequency by 4 for internal use.
LFT	74	-	-	PLL decoupling RCR filter.
RESET/	33	In	-	Master reset Schmitt trigger input, active low. RESET/ should be held low during at least 10ms after power is applied. On the rising edge of RESET/, the chip enters an initialization routine, which may involve firmware download from an external SmartMedia, DataFlash or host.
STIN	34	In Pd	-	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	35	Out	-	Serial test output. 57.6 kbauds async output used for firmware debugging.
PDWN/	31	In	-	Power down input, active low. High level on this pin is typ. VC18. When PDWN/ is low, the oscillator and PLL are stopped, the power switch opens, and the chip enters a deep sleep mode (1 µA typ. consumption when power switch is used). To exit from power down, PDWN/ has to be set high then RESET/ applied. Alternate programmable power-downs are available which allow warm restart of the chip.
TEST	52	In Pd	-	Test input. Should be grounded or left open.

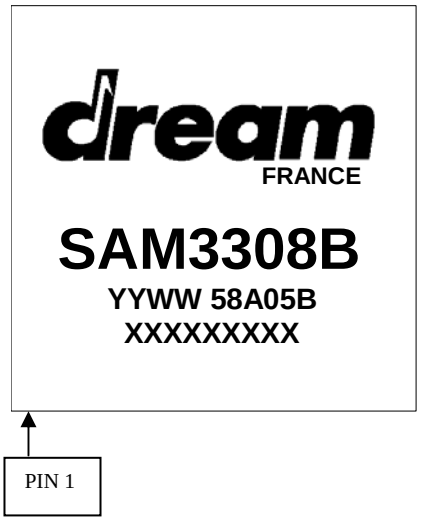
4.2. Pin-out by pin

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	WR/ SMC/ P0.12	**26**	WA7 P2.7	**51**	WA14 P2.14	**76**	D0 I/O0 P0.0 WSAD0
2	RD/ R|B/ P0.13	**27**	WA8 P2.8	**52**	TEST	**77**	D1 I/O1 P0.1 WSAD1
3	WCS1/ P1.10	**28**	PWROUT	**53**	WA15 P2.15	**78**	WD5 P3.5
4	WCS0/ P1.9	**29**	PWRIN	**54**	DAAD0 P0.15	**79**	WD6 P3.6
5	CKOUT	**30**	GND	**55**	DAAD1	**80**	WD7 P3.7
6	CLBD	**31**	PDWN/	**56**	GND	**81**	D2 I/O2 P0.2 WSAD2
7	WSBD	**32**	DFSO	**57**	WA16 P1.0	**82**	D3 I/O3 P0.3 WSAD3
8	IRQ INT/ SMRE/ FS0 P0.8	**33**	RESET/	**58**	WA17 P1.1	**83**	VC33
9	GND	**34**	STIN	**59**	DAAD2	**84**	WD8 P3.8
10	WA0 P2.0	**35**	STOUT	**60**	DAAD3	**85**	WD9 P3.9
11	WA1 P2.1	**36**	WA9 P2.9	**61**	WD0 P3.0	**86**	WD10 P3.10
12	WA2 P2.2	**37**	WA10 P2.10	**62**	WD1 P3.1	**87**	GND
13	VC3	**38**	WA11 P2.11	**63**	WD2 P3.2	**88**	WD11 P3.11
14	WA3 P2.3	**39**	WA12 P2.12	**64**	DABD0	**89**	WD12 P3.12
15	WA4 P2.4	**40**	WA13 P2.13	**65**	DABD1	**90**	D4 I/O4 P0.4 CLAD0

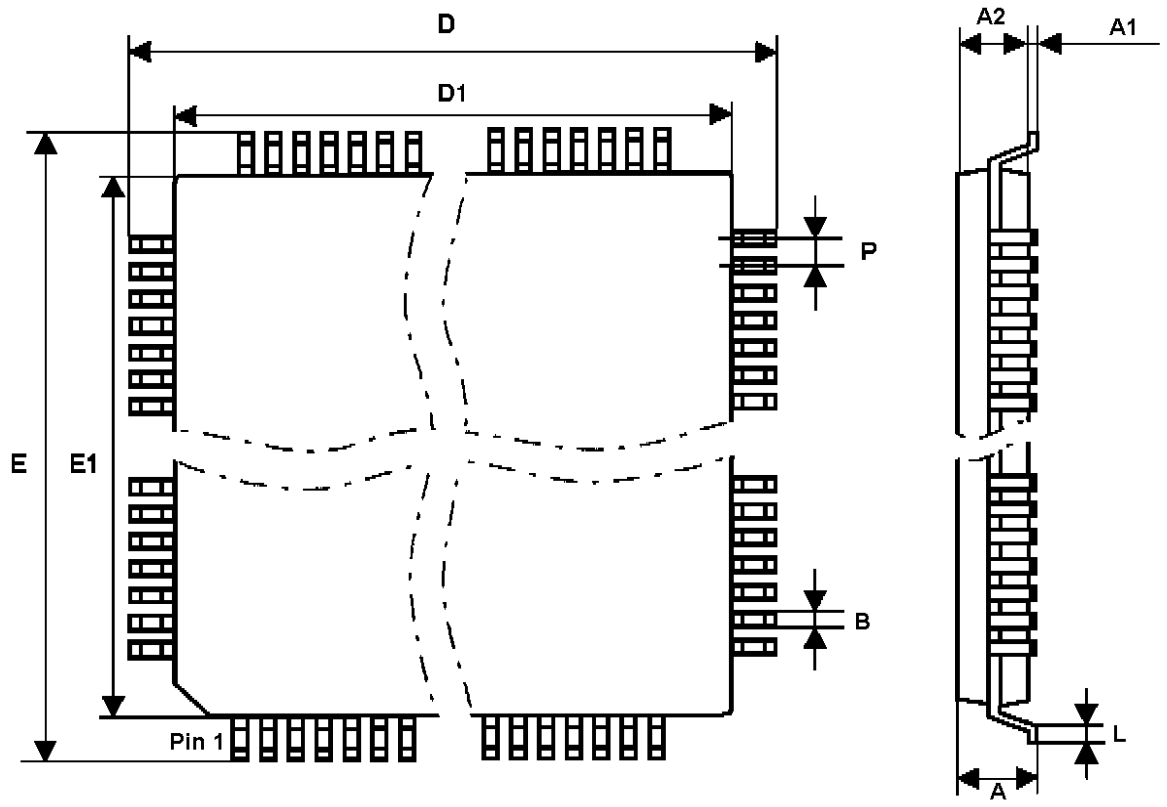
16	WA5 P2.5	**41**	GND	**66**	DABD2	**91**	D5 I/O5 P0.5 CLAD1
17	MIDI_IN P0.14 SDIN	**42**	WA18 SMCLE P1.2	**67**	DABD3	**92**	WD13 P3.13
18	MIDI_OUT FS1 P0.9	**43**	WA19 SMWE/ P1.3	**68**	WD3 P3.3	**93**	WD14 P3.14
19	MUTE P1.6	**44**	WA20 SMALE P1.4	**69**	WD4 P3.4	**94**	WD15 P3.15
20	VC18	**45**	WA21 SMCE/ P1.5	**70**	GND	**95**	D6 I/O6 P0.6 CLAD2
21	WA6 P2.6	**46**	P1.15	**71**	X2	**96**	D7 I/O7 P0.7 CLAD3
22	GND	**47**	VC18	**72**	X1	**97**	GND
23	DFCS/	**48**	WOE/ P1.8	**73**	VC18	**98**	A0 SMPD P0.10 SCLK
24	DFSCK	**49**	WWE/ P1.7	**74**	LFT	**99**	VC18
25	DFSI	**50**	VC33	**75**	GND	**100**	CS/ P0.11 SYNC

5. Marking

LQFP100



6. Mechanical dimensions



SAM3308B
Thin plastic 100 lead quad flat pack (LQFP100)
Dimensions (mm)

	MIN.	NOM.	MAX.
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
L	0.45	0.60	0.75
D		14.00	
D1		12.00	
E		14.00	
E1		12.00	
P		0.40	
B	0.13	0.18	0.23

7. Electrical Characteristics

7.1. Absolute Maximum Ratings(*)

Parameter		Symbol	Min	Typ	Max	Unit
Ambient temperature (Power applied)		-	-40	-	+85	°C
Storage temperature		-	-65	-	+150	°C
Voltage on any pin	X1, LFT	-	-0.3	-	VC18+.3	V
	Others	-	-0.3	-	VC33+.3	V
Supply voltage		VC18	-0.3	-	1.95	V
		VC3	-0.3	-	3.6	V
Maximum IOL per I/O pin		-	-	-	4	mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VC18	1.65	1.8	1.95	V
Supply voltage (note 1)	VC33	3	3.3	VC18+1.5 3.6	V
Supply voltage PWRIN pin	PWRIN	1.75	1.9	1.95	V
Operating ambient temperature	tA	0	-	70	°C

Note 1: Operation at lower VC33 values down to VC18 is possible, however external timing may be impaired. Please contact Dream if you plan to use these circuits with VC33 outside the recommended operating range.

7.3. D.C. Characteristics (TA=25°C, VC18=1.8V±10%, VC33=3.3V±10%)

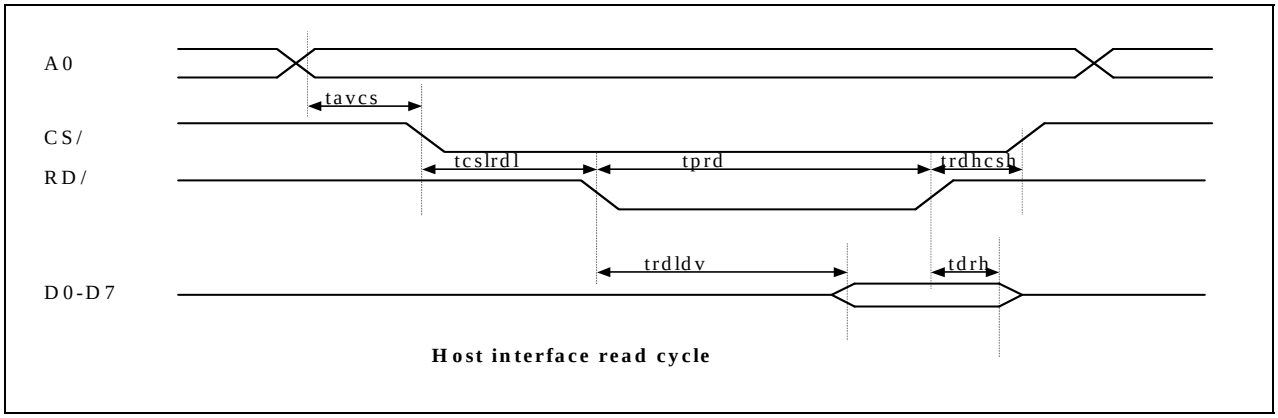
Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-0.3	-	1.0	V
High level input voltage, except X1, PDWN/	VIH	2.3	-	VC33+0.3	V
High level input voltage X1, PDWN/	VIH	1.2	-	VC18+0.3	V
Low level output voltage IOL=-2mA	VOL	-	-	0.4	V
High level output voltage IOH=2mA	VOH	2.9	-	-	V
VC18 power supply current (crystal freq.=11.2896 MHz, all 8 P24 running)	ICC1	-	63	-	mA
VC18 power supply current (crystal freq. = 11.2896 MHz, all P24 stopped)	ICC2	-	22	-	mA
VC18 power supply current (crystal freq. = 11.2896 MHz, all P24 stopped, warm start power-down active)	ICC3	-	4	-	mA
VC18 deep power down supply current (using power switch)	ICC4	-	1	10	µA
Built-in pull-up / pull-down resistor	PU/PD	10	-	56	kOhm

8. Peripherals and Timings

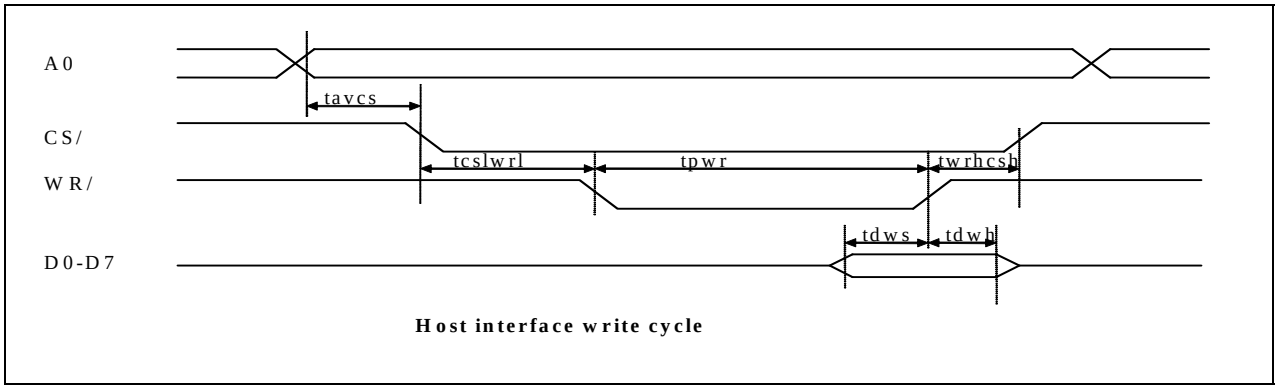
8.1. Slave 8bit parallel interface

Pins used: D7-D0 (I/O), CS/ (input), A0 (input), WR/ (input), RD/ (input), IRQ (output)
This interface is typically used to connect the chip to an host processor.

- Timings



Host interface read cycle



Host interface write cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ low	tcslrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	5	-	-	ns
RD/ pulse width	tprd	50	-	-	ns
Data out valid from RD/	trdldv	-	-	20	ns
Data out hold from RD/	tdrh	5	-	10	ns
Chip select low to WR/ low	tcslrwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	5	-	-	ns
WR/ pulse width	tpwr	50	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0	-	-	ns

- IO Status Register

TE	RF	X	X	X	X	X	X

Status register is read when A0 = 1, RD/ = 0, CS/ = 0

TE: Transmit empty. If 0, data from SAM3308B to host is pending and IRQ is high. Reading the data at A0=0 will set TE to 1 and clear IRQ.
RF: Receiver full. If 0 then SAM3308B is ready to accept DATA from host.

Note: If status bit RF is not checked by host, write cycle time should not be lower than 3µs.

8.2. SmartMedia and other peripheral interface

This is a master 8 bit parallel interface, allowing connection to SmartMedia or other peripherals such as LCD screens.

Pins used:
I/O7-I/O0 (I/O)
SMPD (input)
SMCE/, SMALE, SMCLE, SMRE/, SMWE/ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

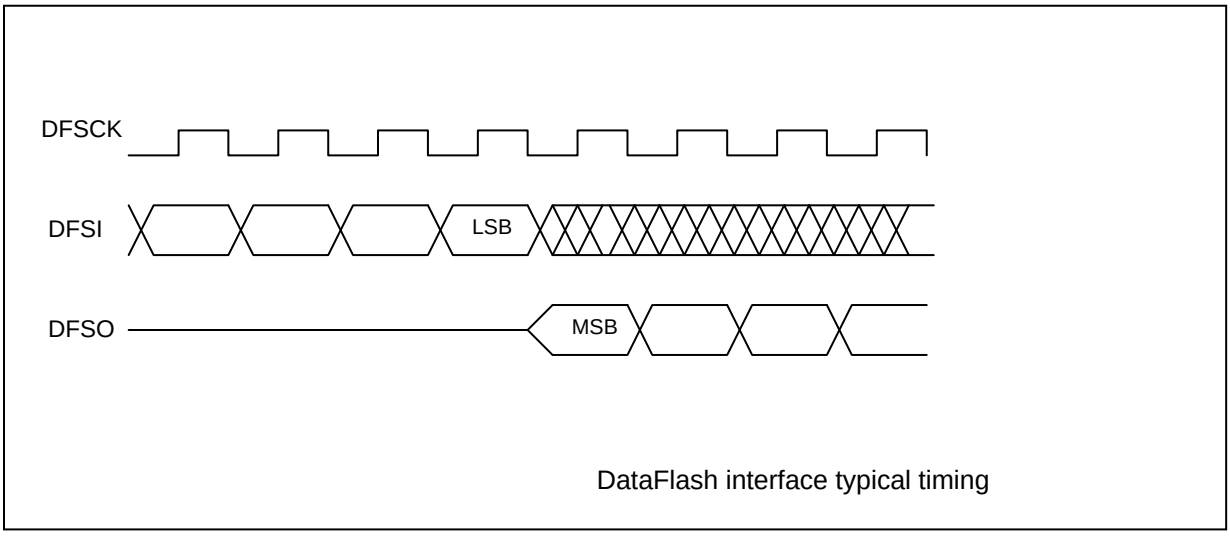
8.3. EEPROM / DataFlash interface

This is a master synchronous serial interface, operating in SPI mode 0.

Pins used:
DFCS/, DFSI, DFSCK (outputs)
DFSO (input)

The DFSCK frequency is firmware programmable from fck to fck/64, fck being the crystal frequency. This allows accommodating a large variety of EEPROM/DataFlash devices.

Please refer to Atmel DataFlash datasheets for accurate SPI mode 0 timing.



DataFlash interface typical timing

8.4. Serial slave synchronous interface

The SAM3308B can be controlled by an external host processor through this unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface. Therefore an external ROM/Flash/EEPROM is required.

Pins used:
SCLK, SYNC, SDIN (input)
INT/ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

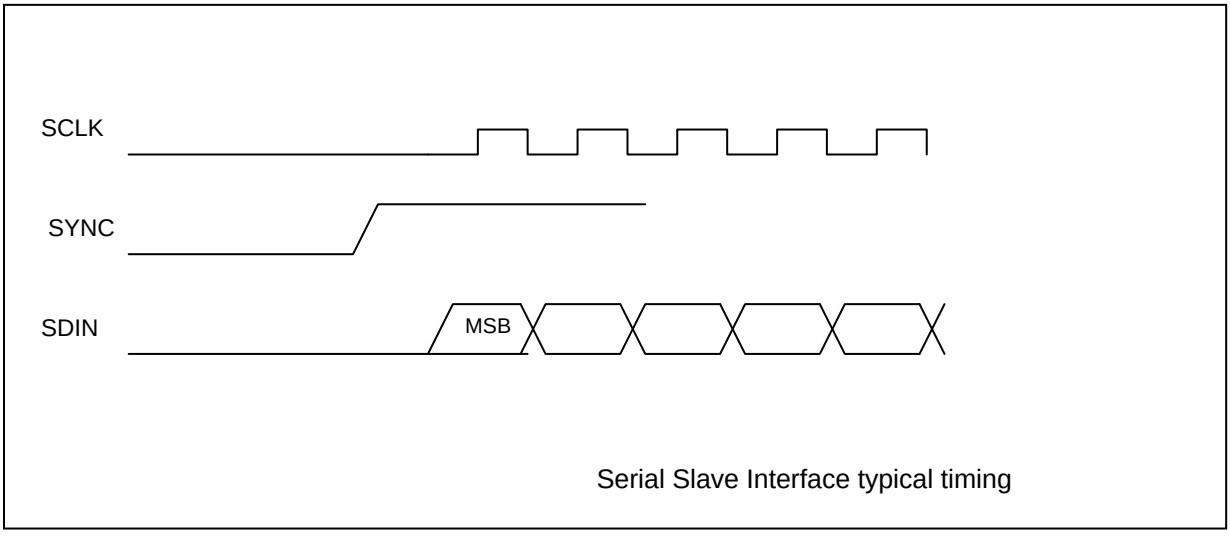
SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN will hold MSB data on the next rising SCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependant. Minimum size is 128 bytes. Host should stop sending data as soon as INT/ goes high.

When the FIFO count is below 64, the INT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SCLK frequency is fck (fck being the crystal frequency).
The minimum time between two bytes is 64 fck periods.

The contents of the SDIN data are defined by the firmware.



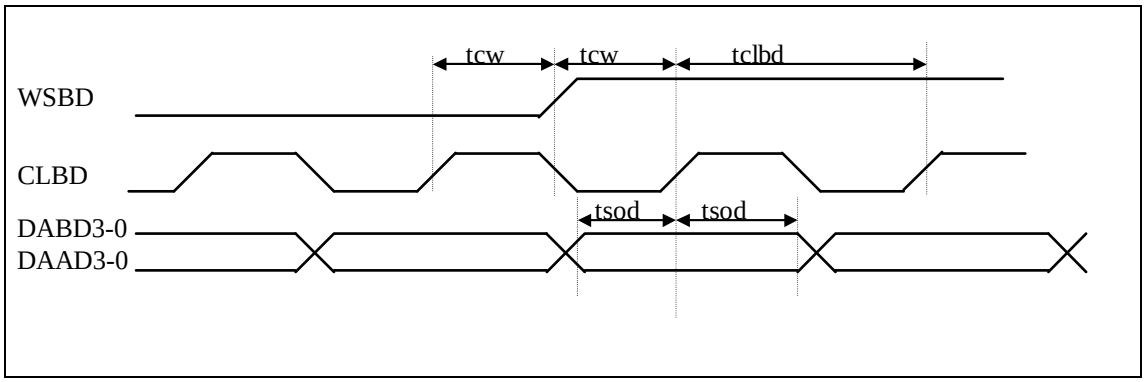
Serial Slave Interface typical timing

8.5. Digital audio

Pins used:
CLBD, WSBD (outputs)
DABD3-0 (outputs)
DAAD3-0 (inputs)
CLAD3-0, WSAD3-0 (inputs)

The SAM3308B allows for 8 digital audio output channels and 8 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD3-0 inputs can be synchronized with incoming CLAD3-0 and WSAD3-0 signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S standard, with up to 24 bits per sample



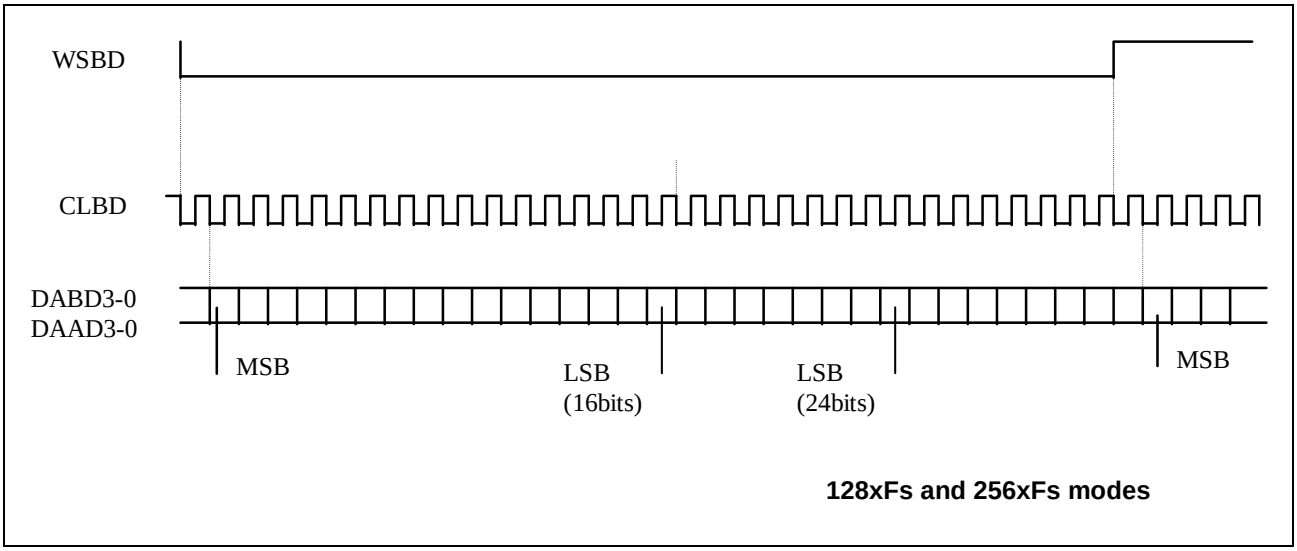
Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	tc-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	tc-10	-	-	ns
CLBD cycle time	tclbd	-	2*tc	-	ns

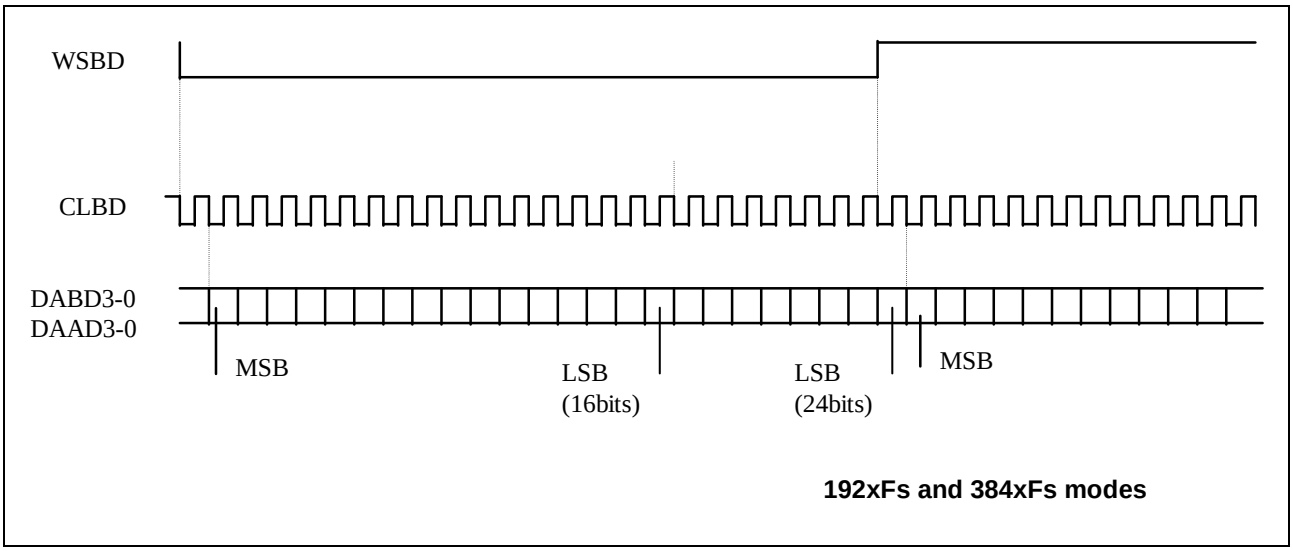
tc is related to tck, the crystal period at X1 as follows:

Sample freq WSBD	Typ Sample Freq	tc	CLBD/WSBD freq ratio
1/(tck*128)	96kHz	tck	64
1/(tck*192)	64kHz	2*tck	48
1/(tck*256)	48kHz	2*tck	64
1/(tck*384)	32kHz	4*tck	48

The choice of sample frequency is done by the firmware.

DIGITAL AUDIO FRAME FORMAT





8.6. Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

baud rate: programmable, typically 31.25 kb/s
format: start bit(0), 8 data bits, stop bit(1)

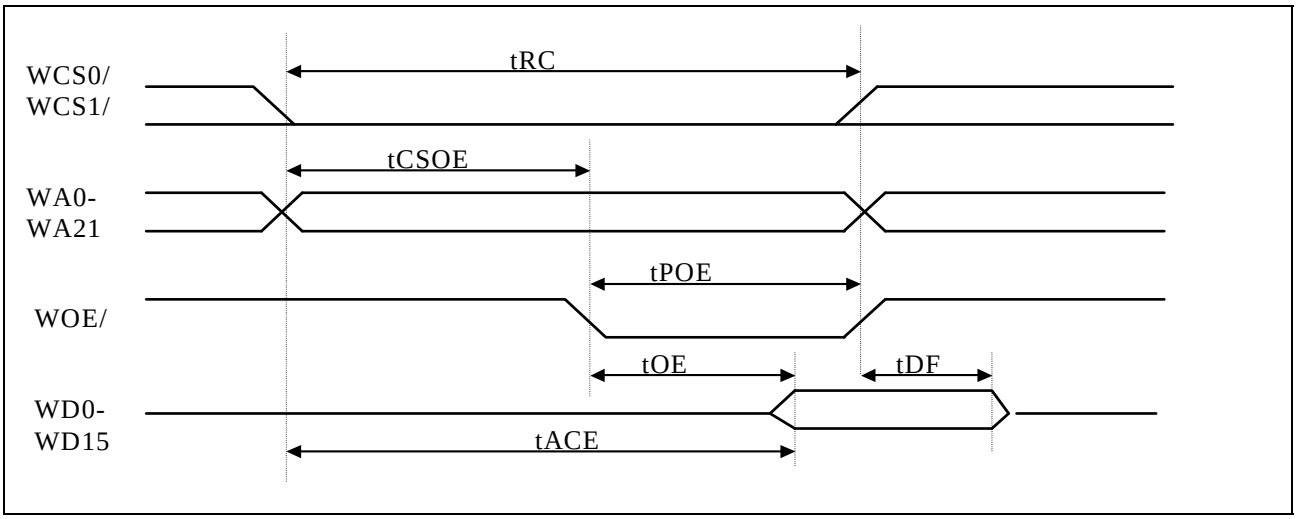
8.7. External memory

Pins used:

WA21-WA0: address out
WD15-WD0: data bi-directional
WCS0/, WCS1/: pre-decodes out
WOE/: output enable
WWE/: write

When using all address bits, the maximum addressing range is two pages (WCS0/, WCS1/) of 4M words (total = 16 Mbytes).

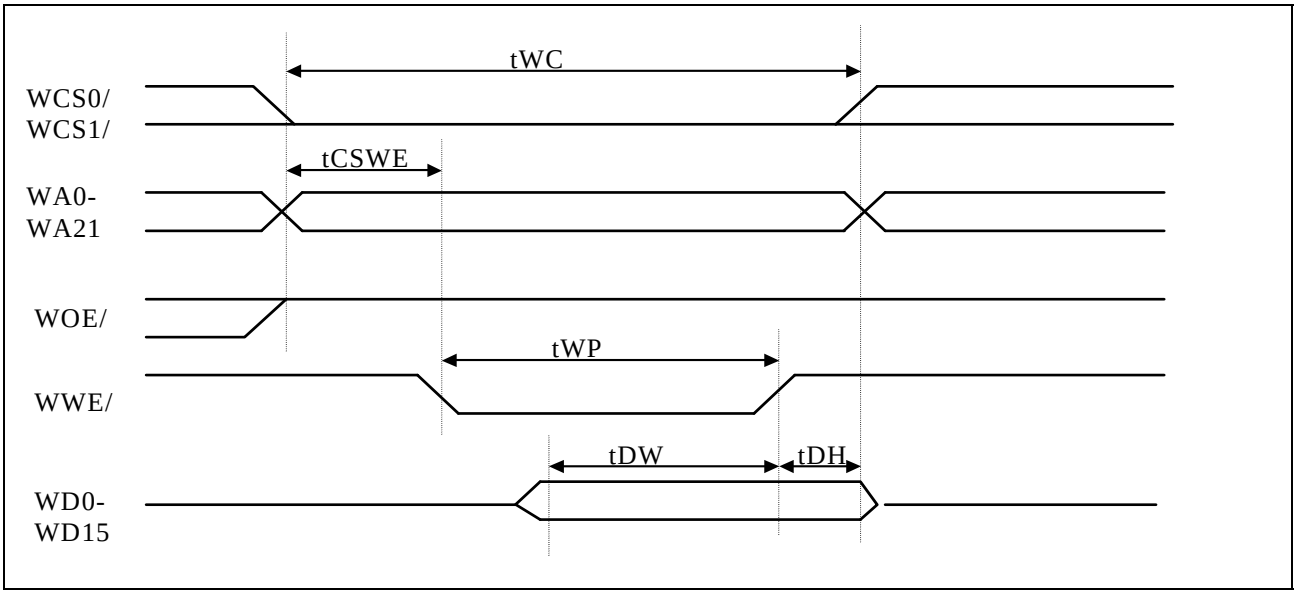
ROM/Flash READ CYCLE



Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	-	5*plck	-	ns
Chip select low / address valid to WOE/ low	tCSOE	2*plck-5	-	2*plck+5	ns
Output enable pulse width	tPOE	-	3*plck	-	ns
Chip select/address access time	tACE	4.5*plck-10	-	-	ns
Output enable access time	tOE	2.5*plck-10	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*plck-5	ns

Notes:
- A built-in PLL multiplies the Xtal clock frequency by 4 for internal use. plck is the period of the internal clock generated by PLL. plck = tck/4. Typical value with Xtal 12.288 MHz is plck = 20 ns.
- Memory access time should be lower than tACEmin. Typical value with Xtal 12.288 MHz is 80ns.

EXTERNAL RAM/FLASH WRITE TIMING



Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	tWC	-	5*plck	-	ns
Write enable low from CS/ or Address or WOE/	tCSWE	2*plck-5	-	2*plck+5	ns
Write pulse width	tWP	-	2.5*plck	-	ns
Data out setup time	tDW	2.5*plck-5	-	-	ns
Data out hold time	tDH	0.5*plck	-	-	ns

9. Reset and Power Down

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.
After the low to high transition of RESET/, following happens:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Addresses 0 &1 from external ROM are checked. If “DR” is read, then control is transferred to address 400H from external ROM.
- SMC/ is sensed. If LOW, then the built-in loader waits for SmartMedia presence detect (SMPD). When detected, the firmware is downloaded from SmartMedia reserved sector 1 and started.
- An attempt is done to read the first two bytes of an external EEPROM or DataFlash. If “DR” is read, then the built-in loader loads the firmware from the external EEPROM/DataFlash and starts it.
- Firmware download from an host processor is assumed.
  1. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip is ready to accept program download. Higher speed transfer can be reach by polling the parallel interface status (CS/=0, A0=1, RD/=0).
  2. The host sends the firmware size (in words) on two bytes (Low byte first).
  3. The host sends the SAM3308B firmware. The firmware should begin with string ”DR”.
  4. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip has accepted the firmware.
  5. SAM3308B starts the firmware.

If PDWN/ is asserted low, then the crystal oscillator and PLL will be stopped. If the power switch is used, then the chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256

10. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VC33, VC18 distribution, decoupling

All GND, VC33, VC18 pins should be connected. A GND plane is strongly recommended. The board GND + VC33 distribution should be in grid form.

Recommended VC18 decoupling is 0.1µF at each corner of the IC with an additional 10µFT decoupling close to the crystal. VC33 requires a single 0.1µF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the IC should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from the IC.

- Busses

Parallel layout from D0-D7 and WA0-WA21/WD0-WD15 should be avoided. The D0-D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA21/WD0-WD15 which can corrupt address and/or data on these busses.

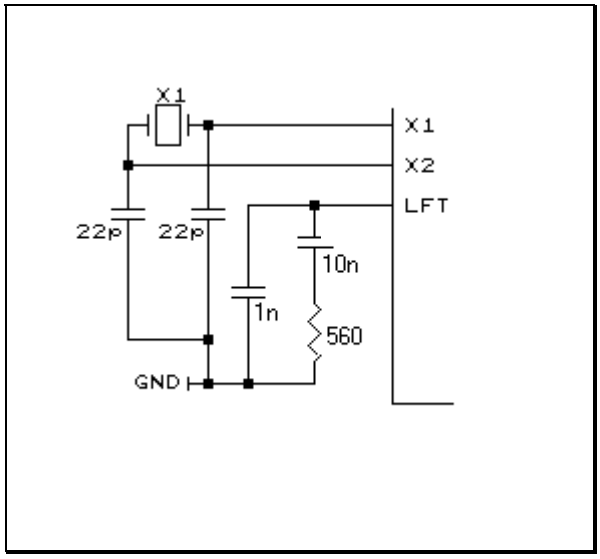
A ground plane should be implemented below the D0-D7 bus, which connects both to the host and to the IC GND.

A ground plane should be implemented below the WA0-WA21/WD0-WD15 bus, which connects both to the ROM/Flash grounds and to the IC.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

11. Recommended Crystal Compensation and LFT Filter



12. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (98, ME, 2000, XP). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program Flash, Dataflash, EEPROM, SmartMedia on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. This allows very quick time to market by testing directly into the final prototype.

A library of frequently used functions is/will be available such as:

- Wavetable synthesis
- Reverb/Chorus
- MP3 decode
- Sample rate conversion
- 31 band equalizer
- Parametric equalizer

Dream engineers are available to study customer specific applications.

Dream Contact

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Website

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June 2011