SAM5916B

AUDIO & MUSIC MULTI-DSP PROCESSOR

Key features

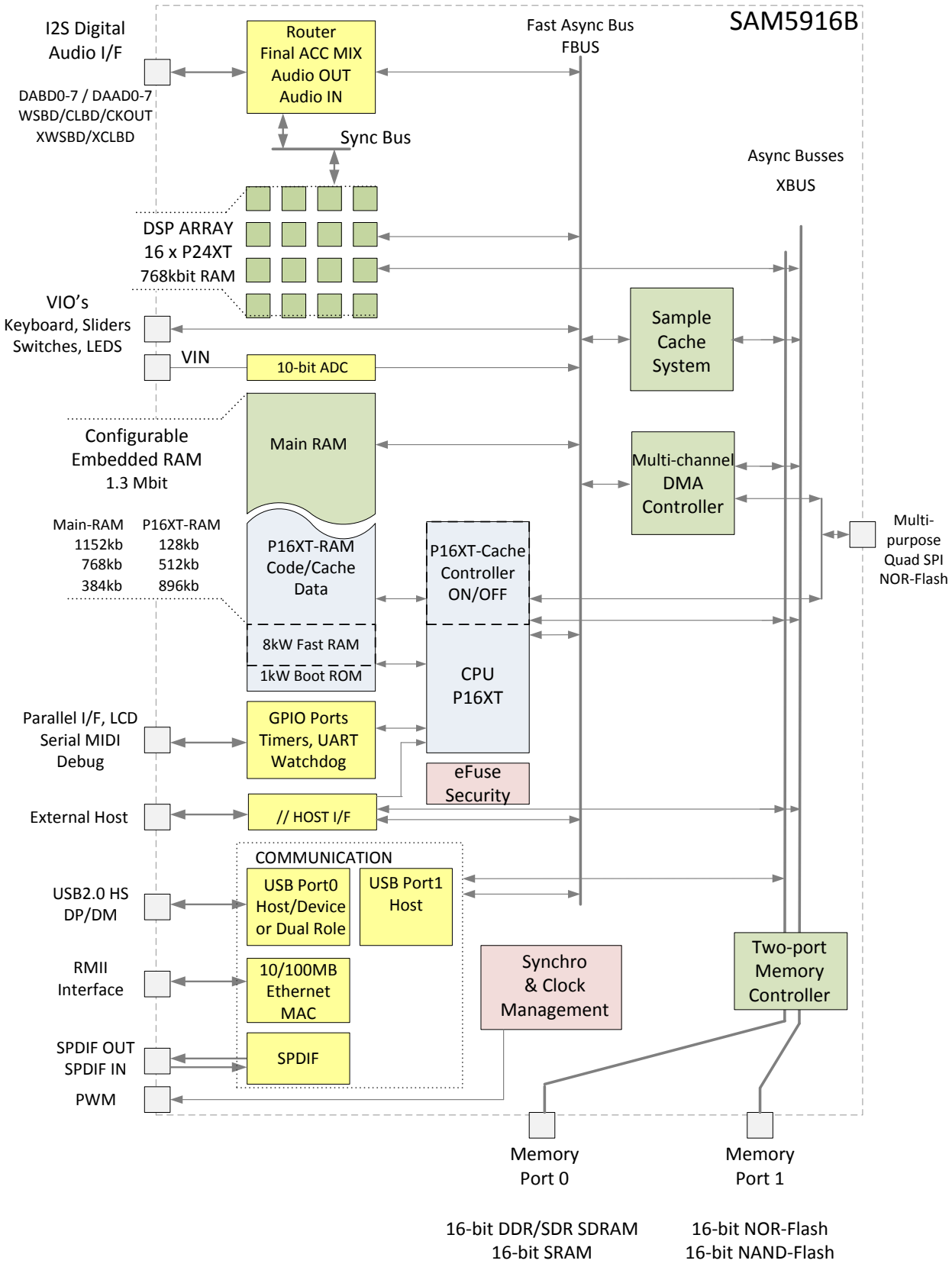
- **Dream DSP Array of 16 new 24bit/56bit DSP cores** (P24XT) supporting 56bit MAC operations (800M MAC/sec), vector processing, double precision instructions and offering a rich set of hardware accelerated macro-instructions (including 48x48bit multiply, double precision bi-quad filter)
- New highly **speed optimized 16bit CPU** (P16XT) with optimized instruction set for C compiler, interrupts, new fast 32-bit instructions, 512Kword max. program code size
- Built-in 1kbit eFuse for configuration and security (program code and sound bank protection)
- Built-in configurable fast **Data/Effect RAM up to 48Kx24** (or 72Kx16), + 32Kx24 DSP RAM
- Built-in configurable fast Program Code/Cache RAM, on-the-fly program code decryption
- Multi-channel DMA for fast data transfers to external memories, supports circular buffers and transparent 24- to 16-bit transformation
- External memories: **2 separated parallel memory ports** with flexible configurations (NOR Flash + SRAM/SDR/DDR, 16bit or 8bit SLC NAND Flash (with ECC) + SDR/DDR), up to 1.5GByte addressing space for NOR Flashes, **8GByte for NAND Flashes**
- On-the-fly wave sample decryption (AES encryption format with high security)
- 8-bit or 16-bit parallel slave Port for external Host control and fast data transfer
- Multi-purpose SPI interface (single or Quad-SPI, mode 0) for Serial Flash, SD-Card, etc.
- Serial MIDI IN/OUT interface (optional 2nd I/F)
- **Two USB 2.0 High Speed Ports** (HOST, DEVICE or Dual-Role)
- **10/100 Mbps Ethernet MAC** with RMII interface to external PHY
- **S/PDIF interface** (IEC60958) with clock recovery (concurrent IN/OUT)
- Up to 16 Audio channels IN, 16 Audio channels OUT, all Audio IN can be used in clock slave mode
- Watchdog, Timers, Power reduction modes, unused primary interfaces can be used as GPIOs
- 216-pin LQFP package

Typical applications

- High-Range Digital Pianos, Keyboards & Sound modules

1. SAM5916B Internal Architecture

1.1. Block Diagram



1.2. Overview

Based on a multi-layer architecture, the new family of DREAM's Audio & Music processors (SAM5000) is built around a new highly speed optimized 16-bit CPU (P16XT) and a configurable array of hardware accelerated 24-bit DSP cores (P24XT).

A Sample Cache System dedicated to sound synthesis allows SAM5000 processors to reach high levels of polyphony whatever the memory type used for sound bank storage. Moreover, this solution allows on-the-fly decryption of waves protected with strong AES(*) encryption.

The processing of delay lines in external memory is hugely facilitated with the integration of a multi-channel DMA controller. This controller performs fast memory-to-memory data transfers with some key features: burst modes and circular buffer structures are supported and data are automatically re-formatted (24-bit↔16-bit) when transfers are done from internal to external memories. Transfers can be done in parallel on several channels without requiring any assistance of the CPU or DSP cores.

The SAM5916B is part of the new generation of DREAM's audio & music processors and automatically inherits all above features. With an array of 16 P24XT DSP cores, the SAM5916B offers high performance processing. Delivered in a 216-pin QFP package offering a maximum of connectivity, it is mainly intended for piano and keyboard applications requiring high quality sound synthesis and effect processing.

In addition to a large variety of communication interfaces (USB 2.0 HS ports, Ethernet MAC controller, S/PDIF IN/OUT…), the SAM5916B has two separated memory ports. More bandwidth can be obtained in various memory configurations: SDR/DDR SDRAM or SRAM devices on Port 0, and NOR-Flash or SLC NAND-Flash devices for the storage of huge sound banks on Port1. Up to 4 different memory configurations can be defined with pull-resistors externally connected to dedicated pins. Memory configuration is read by boot program at power-up from dedicated pins or fuse bits.

The SAM5916B includes a 24-bit Audio Router and supports up to 16 Audio Channels IN & OUT. Depending on primary functions in use, digital audio signals can be accessed via primary or secondary IO pads. Most of the IO pads that are not used for primary functions remain available for secondary functions or for firmware programmable IO functions (Versatile IO's or GPIO's).

The SAM5916B can handle up to 176 switches (organized in matrix form) and 88 LEDs (in a time multiplexed way) through versatile firmware programmable IO pads. Keyboard and switches scanning tasks can be fully customized in one dedicated P24XT, making the SAM5916B directly compatible with most of velocity keyboards. Similarly, LCD or graphic displays can be directly connected to programmable IO's and controlled by the P16XT.
A built-in ADC allows connecting continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc.

A built-in 1kbit eFuse provides a plenty of irreversible One-Time-Programmable bits for the storage of configuration parameters, decryption keys and other security purposes. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5916B.

(*) AES is the worldwide most used symmetric-key algorithm.

1.3. DSP Array – 16 * P24XT

The SAM5916B is built around an Array of 16 new 24-bit DSP cores (P24XT).

Similarly to previous generation, each P24XT DSP core includes a 2k x 24 RAM and a 2k x 24 ROM. The RAM contains both data and DSP instructions, while the ROM contains typical coefficients such as FFT cosines and windowing and micro-code for hardware accelerated micro-instructions.

The P24 sends and receives audio samples through the Sync Bus at the frame rate (typically, 48kHz frame period = 2048 cycles at 98.8 MHz). For the transfer of all other data, the P24XT is able to communicate in an asynchronous way through Async Busses. P24XT memories can be accessed through the Async Bus by others.

A lot of operations can be performed with much more precision with new P24XT core.
For single-precision operations:

- Programmable 24-bit fixed format: 1.0.23, 1.2.21, 1.8.15 or 1.15.8
- 56-bit MAC unit with 24-bit x 24-bit multiplication + 8 guard bits to prevent overflow issues

For double-precision operations:

- Programmable 48-bit fixed format: 1.0.47, 1.2.45, 1.8.39 or 1.15.32
- Large set of 48-bit Double Precision (DP) operations

The P24XT DSP core also offers hugely improved performances with a new and rich set of hardware accelerated macro-instructions:

  - ADD, MUL, MAC operations on vectors can be performed with only one macro-instruction, address pointers being self-incremented
  - ring buffer structures are supported in several vector instructions
  - several arithmetic operations are available: SIN, COS, DIV, LN, EXP, …
  - Operations on complex values in single and double precision
  - Polynomial calculation in single and double precision
  - Optimized filtering instructions: 1^{st} & 2^{nd} order filters, programmable number of taps, single or double precision

Based on polynomial interpolation, up to 24 voices (at typical 48kHz frame clock) with high quality filtering can be synthesized within one P24XT, and up to 50M of 56-bit MAC operations can be performed per second.

1.4. Sync Bus

The Sync Bus transfers audio samples on a frame basis, typical frame rates being 44.1, 48, 96 & 192 kHz. Each frame is divided into 32 time slots. Each slot is divided into 8 bus cycles. Each P24XT is assigned a hardwired time slot (16 to 31), during which it may provide 24-bit data to the bus (up to 8 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 15 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

1.5. Async Busses

As shown in the general block diagram, several 24-bit Async Busses can be accessed by most of masters (P16XT, P24XT, DMA controller…) in a parallel way. Two busses XBUS0 & XBUS1 give access to external memories.

1.6. Enhanced 16-bit CPU – P16XT

The SAM5916B operates under the control of a new highly speed optimized 16-bit CPU (P16XT).

The key features of the P16XT are the following:

- Operating frequency up to 196.6 MHz
- New instructions including 32 bit data handling and 32x32 multiply
- Maximum executable program size = 512k words
- Backward compatibility with previous P16 products and optimized instruction set for C-compiler
- Interrupt handling: 3 interrupt signals, 32 sources with programmable Mask, Polarity & Triggering mode

A tightly coupled code/cache memory allows the P16XT to fetch code lines with reduced latency when needed. This memory can be either used as code memory when the whole firmware can be stored in internal memory or as cache memory (n-Way Set Associative Cache System) in other cases. The internal code/cache memory is loaded during the boot sequence (at power-up) by P16XT ROM boot program.

By default, the code/cache memory has a size of 512kbits (32k*16). Depending on performance requirements, the distribution of internal memory between code/cache and data/effect partitions can be modified as explained in the next paragraph.

The P16XT ROM holds the boot program as well as a debugger which uses a dedicated asynchronous serial line.

1.7. On-chip memory

Besides distributed memory in P24XT DSP cores (16 * 2Kx24-bit RAM for a total of 768kbits) and in communication controllers, the SAM5916B offers 1.4M bits of on-chip memory. One part of this memory (P16XT-RAM) is reserved for direct access by the P16XT (tightly coupled code/cache memory). The second part of this memory (MAIN-RAM) is used as data memory and can be accessed by any master through the asynchronous bus.

The memory partitioning is configurable by firmware. The memory space is divided into 4 banks:

- Bank 0 has a size of 256kbits and is accessed by P16XT only.
- Banks 1 & 2 have a size of 384kbits and can be either used as code/cache memory for P16XT or as main data memory
- Bank 3 has a size of 384kbits and is always used as main data ram

		RAMCFG='00'		RAMCFG='01'		RAMCFG='10'	
		P16XT RAM	Main RAM	P16XT RAM	Main RAM	P16XT RAM	Main RAM
Bank0	256 kbits	16kx16	-	16kx16	-	16kx16	-
Bank1	384 kbits	-	16kx24	24kx16	-	24kx16	-
Bank2	384 kbits	-	16kx24	-	16kx24	24kx16	-
Bank3	384 kbits	-	16kx24	-	16kx24	-	16kx24
Total		256kbits 16kx16	1152kbits 48kx24	640kbits 40kx16	768kbits 32kx24	1Mbits 64kx16	384kbits 16kx24

1.8. Multi-channel DMA controller

The DMA controller is intended to perform high-speed memory-to-memory data transfers without using CPU resources: blocks can be copied from one source address to one destination address with a specified length, while both source and destination addresses are self-incremented. Taking advantage of the multi-layer architecture, this module can operate on several channels in parallel. Moreover, the DMA controller is able to automatically perform 24-bit to 16-bit transformation when data blocks are transferred from internal to external memories. For making the handling of delay lines easier, circular buffers are also supported.

Main features:

- The DMA controller has 4 channels
- programmable block length and source & destination addresses
- supports word and burst transfers
- supports ring buffers
- transparent 24-bit to 16-bit transformation

1.9. Sample Cache System

Thanks to its sample cache system, the SAM5916B can support up to 256 voices of polyphony with sound banks stored either in SDR/DDR, NOR-Flash or in NAND-Flash. With NAND-Flash, cache memory must be extended in external SDR/DDR.

1.10. Two-port memory controller

The two-port memory controller enables the SAM5916B to interface with several memory types:

- 16-bit DDR-SDRAM, SDR-SDRAM or SRAM on Port 0
- 16-bit NOR Flash or 16-bit NAND Flash on Port 1

For the storage of sound banks, address lines support

- up to 4 x 256MBytes (or 3 x 512MBytes) of non-volatile NOR Flash memory
- up to 2 x 4GBytes of non-volatile NAND Flash memory

4 different memory configurations are defined with pull-resistors externally connected to dedicated pins. Memory configuration is read by boot program at power-up from dedicated pins or fuse bits. Possible memory configurations are the following:

Config	*Port0*	*Port1*
1	16-bit SDR/DDR	16-bit NOR Flash
2	16-bit SRAM	16-bit NOR Flash
3	16-bit SDR/DDR	16-bit SLC NAND Flash (with ECC solution)
4	16-bit SDR/DDR	8-bit SLC NAND Flash (with ECC solution)

The two-port memory controller handles transfer requests initiated by masters like P16XT CPU, P24XT DSP cores, DMA controller, Sample cache system or other communication controllers through both XBUS asynchronous busses.

Control registers are accessed by the P16XT for defining configuration and optimizing frequency and latency parameters. Burst transfers are always initiated when possible.

1.11. Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 16 channels of audio in and 16 channels of audio out are provided (8 stereo in/out, I2S or MSB Left format). The stereo audio in channel may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

1.12. External Host Interface

The Host Parallel Interface is used for fast read/write transfers between an external host processor and the SAM5916B. E.g. it allows an external host to be a master for fast data transfer to SAM5916B connected memories (the handshake protocol for the fast data transfer is driven by the firmware).
This module is connected internally to asynchronous busses.

1.13. Versatile I/O's and GPIO's

Most of the IO pads, when not used for primary (or secondary) specific functions, remain available as firmware programmable IO pads. Programmable IO functions are divided into 2 categories:

- Versatile IO's when they can be controlled through asynchronous busses by either P16XT or P24XT cores for keyboard scanning, sliders, switches and LED's control.
- General Purpose IO's (GPIO's) when accessible by the P16XT only for functionalities like LCD Display control, …

1.14. High-speed USB 2.0 – Ports 0 & 1

USB Port 0 allows the SAM5916B to connect it directly to

- a USB host such as a PC in device mode
- a USB device such as a mass storage USB key in host mode.
- USB Port 0 supports also dual-role mode

USB Port 1 is used in host mode.

Both USB Ports 0 & 1 have PHY on-die.

1.15. 10/100Mbit Ethernet MAC

The SAM5916B offers the capability to be directly connected to a network by way of an embedded Ethernet MAC. The controller supports both 10M and 100M bits/sec. Low-pin count RMII protocol is used for connection to external PHY.

1.16. S/PDIF – Sony/Philips Digital Interface

The S/PDIF audio module allows the SAM5916B to receive and transmit digital audio concurrently. The SAM5916B provides one single S/PDIF receiver with an input signal and one S/PDIF transmitter with another output signal.

For synchronization purposes, the audio clock can be recovered from the incoming audio stream.

1.17. Synchronization and clock management

Depending on the application, the SAM5916B supports 3 clock sources (OSC1, OSC2 & VCXO) for the generation of the reference clock (see table below) and 2 programmable PLL. With a crystal at 12.288MHz, the main PLL generates a clock at 393.2 MHz (32*12.288MHz). This high-frequency system clock is optionally divided through programmable dividers to generate several slower control clocks. Most of internal clocks can be stopped individually for flexible power optimization.

For audio streaming applications, the SAM5916B is able to behave as a slave. Synchronization to an external clock, extracted from input audio streaming for example, can be achieved by controlling an external VCXO with built-in PWM signal. Re-synchronized clock from VCXO can be used as 3rd clock source. In this case, the SAM5X does use the clock from OSC1 (12MHz) during the start-up period.

Clock Mode	USB/ Eth in use	Description	OSC1 (MHz)	OSC2 (MHz)	Audio Source Clock (MHz)	Typical (*) frame clock (kHz)
0	Yes	Single-Xtal 12MHz-USB/Eth	12	NU	12	46.875
1	No	Single-Xtal 12.288/11.2896MHz-Audio	12.288 11.2896	NU	12.288 11.2896	48 44.1
2	Yes	Two-Xtal 12MHz-USB/Eth + 12.288/11.2896MHz-Audio	12	12.288 11.2896	12.288 11.2896	48 44.1
3	Yes	Two-Xtal 12MHz-USB/Eth + VCXO	12	VCXO	VCXO	Ext. frame frequency

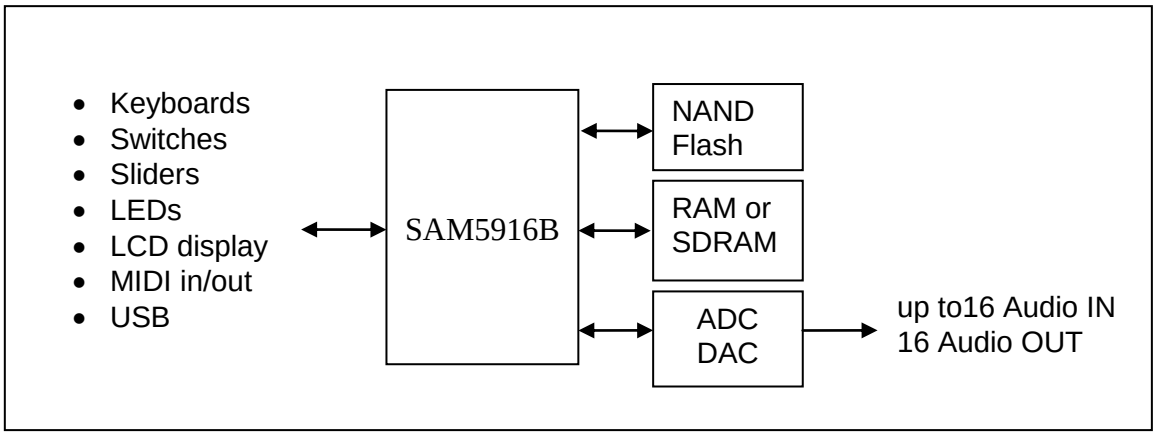
(*)SAM5000 supports 46.875kHz, 48/44.1KHz, 96/88.2KHz and 192KHz sampling rates

1.18. eFuse and security

A built-in 1kbit eFuse provides a plenty of irreversible One-Time-Programmable bits for the storage of configuration parameters, decryption keys and other security purpose data. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5916B.

2. Typical application examples

2.1. **High Range Piano / Keyboard** (using Memory Configuration 3 or 4)



- Up to **256-voice** high quality sound synthesis (polynomial interpolation, new filter modes…)
- Copy protected sound banks cost saving memories (NAND Flash + SDRAM)
- Independent simultaneous high quality Effects Processing blocks:
  - New high-class Reverb
  - Chorus/Flanger/Phaser/Tremolo/Rotary
  - Amp-Modeling (Distortion), Compressor
  - Delay
  - flexible Equalizers for cabinet corrections and modelling, and user EQ settings
  - Sympathetic String/Pedal Resonance for high range digital Piano products
  - …and many others out of vast Dream Effect Library
- Direct connection to keyboard, switches, LEDs, Graphic LCD display
- 10-bit ADC for continuous controllers like sliders and pedals
- Two independent USB 2.0 High-Speed Ports can be used for concurrent
  - USB-to-Host: Audio Class compliant Audio/MIDI interface to a computer
  - USB-to-Device: USB-Stick / Flash drive for song playback and data storage etc.

3. SAM5916B capacity and I/O configuration

The SAM5916B can run a firmware from an external NOR Flash, Quad-SPI NOR Flash, NAND Flash or serial SPI-Flash/DataFlash/EEPROM memory, by using cache mode or boot-load mechanism. A firmware can also be down-loaded from a Host CPU, and SAM5916B runs the firmware from local RAM. The SAM5916B can use its local RAM for effects processing (the embedded RAM is widely configurable for best choice between program and effects memory space), it can be extended by external low cost SRAM, Quad-SPI RAM or SDRAM. The SAM5916B is the ideal choice for low cost digital piano, keyboards and professional electronic drum products, with low count of required external components and many configurable I/Os.

3.1. DSP considerations

The SAM5916B includes 16 x P24XT DSPs.
The table below lists the performance achievable by the P24:

Function	P24XTs required
256-voice Wavetable Synthesis @48kHz	11
stereo Reverb, Chorus, Equalizer and Keyboard Scanning @48kHz	1

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pin-out to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host-controlled operation

There are 3 main ways of communication with a host processor:

- 8-bit parallel bi-directional Host interface
  signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial (UART), 2x MIDI_IN and 2x MIDI_OUT
- Synchronous serial
  signals: SSDIN, SSCLK, SSYNC, SSINT/

3.2.2. Stand-alone operation

Possible stand-alone modes are:
- Firmware into external parallel NOR Flash
- Firmware into external NAND Flash memory
- Firmware into external SPI NOR Flash connected on Multi-Purpose SPI bus

4. SAM5916B PINOUT

4.1. Memory Config

The SAM5916B can be used in 4 different hardware configurations called Memory Config. This flexible architecture allows selecting the appropriate memory interfaces for each application.

Memory Config can be defined in two ways:
1. Sensed at start-up: Memory Config is defined by the level on MC0 and MC1 pins sensed at start-up. MC0 sensed on CKOUT and MC1 sensed on SPICK.
2. Read from Efuse MC bits: Memory Config is preprogrammed in embedded eFuse. In this case MC0-MC1 pins will not be sensed.

4.1.1. Memory Config Table

MC1	MC0	Memory Config	Description
0	0	1	SDRAM + NOR Flash
0	1	2	SRAM + NOR Flash
1	0	3	SDRAM + NAND 16-bit Flash
1	1	4	SDRAM + NAND 8-bit Flash

4.2. Pin-out by pin

4.2.1. Memory Config 1: SDRAM + NOR Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	55	DRDQ3	109	VD33	163	GND
2	TEST	56	GND	110	VIN	164	CKOUT
3	STIN	57	VC12	111	VA33	165	DABD0
4	STOUT	58	VM	112	AGND	166	DAAD0
5	MIDI_IN1	59	DRDQ4	113	SEL0	167	WA16
6	MIDI_OUT1	60	DRDQ5	114	SEL1	168	WA17
7	SPICK	61	DRDQ6	115	DABD1	169	WA18
8	SPICS0/	62	DRDQ7	116	REF_CLK	170	WWE/
9	VD33	63	DRDQ8	117	CS/	171	WOE/
10	TXD0	64	DRDQ9	118	RD/	172	VD33
11	TXD1	65	VM	119	WR/	173	VD33
12	RXD0	66	DRDQ10	120	IRQ	174	WA8
13	RXD1	67	DRDQ11	121	A0	175	WA9
14	TX_EN	68	DRDQ12	122	D0	176	WA10
15	CRS_DV	69	DRDQ13	123	VD33	177	WA11
16	RX_ER	70	DRDQ14	124	D1	178	WA12
17	ETH_RES/	71	DRDQ15	125	D2	179	WA13
18	ROW0	72	VM	126	D3	180	WA14
19	ROW1	73	DRA4	127	D4	181	WA15
20	ROW2	74	DRA5	128	D5	182	WA0
21	ROW3	75	DRA6	129	D6	183	WA1
22	VD33	76	DRA7	130	D7	184	WA2
23	SPI0	77	DRA8	131	VD12	185	WA3
24	SPI1	78	DRA9	132	MK8	186	WA4
25	SPI2	79	VM	133	MK9	187	VD33
26	SPI3	80	VD12	134	MK10	188	WA5
27	VM	81	DRA10	135	NRCS10/	189	WA6
28	DRCAS/	82	DRA11	136	NRCS11/	190	WA7
29	DRRAS/	83	DRA12	137	NRCS12/	191	WD0
30	DRWE/	84	DRA13	138	NRCS13/	192	WD1
31	DRCKE	85	DRBA0	139	VD33	193	WD2
32	DRCS0/	86	DRBA1	140	WA19	194	WD3
33	DRCS1/	87	VM	141	WA20	195	WD4
34	VM	88	MK0	142	WA21	196	WD5
35	DRCS2/	89	MK1	143	WA22	197	WD6
36	DRCS3/	90	MK2	144	WA23	198	WD7
37	DRA0	91	MK3	145	WA24	199	WD8
38	DRA1	92	MK4	146	WA25	200	VD33
39	DRA2	93	MK5	147	WA26	201	WD9
40	DRA3	94	MK6	148	USBID	202	WD10
41	VM	95	MK7	149	FSOURCE	203	WD11
42	VD12	96	BR0	150	OSC1_X1	204	WD12
43	VD12	97	BR1	151	OSC1_X2	205	WD13
44	DRDS0	98	BR2	152	VD33U0	206	WD14
45	DRDS1	99	BR3	153	USBDM0	207	WD15
46	DRDM0	100	BR4	154	USBDP0	208	VD33O
47	DRDM1	101	BR5	155	GNDU0	209	OSC2_X1
48	DRCK/	102	BR6	156	USBREF0	210	OSC2_X2
49	VM	103	BR7	157	GND	211	GNDO
50	DRCK	104	BR8	158	VD33U1	212	GND
51	VREF	105	BR9	159	USBDM1	213	VC12
52	DRDQ0	106	BR10	160	USBDP1	214	OUTVC12
53	DRDQ1	107	CLBD	161	GNDU1	215	VD33R
54	DRDQ2	108	WSBD	162	USBREF1	216	GNDR

4.2.2. Memory Config 2: SRAM + NOR Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	55	MD3	109	VD33	163	GND
2	TEST	56	GND	110	VIN	164	CKOUT
3	STIN	57	VC12	111	VA33	165	DABD0
4	STOUT	58	VM	112	AGND	166	DAAD0
5	MIDI_IN1	59	MD4	113	SEL0	167	WA16
6	MIDI_OUT1	60	MD5	114	SEL1	168	WA17
7	SPICK	61	MD6	115	SRCS/	169	WA18
8	SPICS0/	62	MD7	116	REF_CLK	170	WWE/
9	VD33	63	MD8	117	MA16	171	WOE/
10	TXD0	64	MD9	118	MA17	172	VD33
11	TXD1	65	VM	119	MA18	173	VD33
12	RXD0	66	MD10	120	MWE/	174	WA8
13	RXD1	67	MD11	121	MOE/	175	WA9
14	TX_EN	68	MD12	122	D0	176	WA10
15	CRS_DV	69	MD13	123	VD33	177	WA11
16	RX_ER	70	MD14	124	D1	178	WA12
17	ETH_RES/	71	MD15	125	D2	179	WA13
18	ROW0	72	VM	126	D3	180	WA14
19	ROW1	73	MA4	127	D4	181	WA15
20	ROW2	74	MA5	128	D5	182	WA0
21	ROW3	75	MA6	129	D6	183	WA1
22	VD33	76	MA7	130	D7	184	WA2
23	SPI0	77	MA8	131	VD12	185	WA3
24	SPI1	78	MA9	132	MK8	186	WA4
25	SPI2	79	VM	133	MK9	187	VD33
26	SPI3	80	VD12	134	MK10	188	WA5
27	VM	81	MA10	135	NRCS10/	189	WA6
28	CS/	82	MA11	136	NRCS11/	190	WA7
29	RD/	83	MA12	137	NRCS12/	191	WD0
30	WR/	84	MA13	138	NRCS13/	192	WD1
31	IRQ	85	MA14	139	VD33	193	WD2
32	DABD3	86	MA15	140	WA19	194	WD3
33	DAAD1	87	VM	141	WA20	195	WD4
34	VM	88	MK0	142	WA21	196	WD5
35	DAAD3	89	MK1	143	WA22	197	WD6
36	P3.7	90	MK2	144	WA23	198	WD7
37	MA0	91	MK3	145	WA24	199	WD8
38	MA1	92	MK4	146	WA25	200	VD33
39	MA2	93	MK5	147	WA26	201	WD9
40	MA3	94	MK6	148	USBID	202	WD10
41	VM	95	MK7	149	FSOURCE	203	WD11
42	VD12	96	BR0	150	OSC1_X1	204	WD12
43	VD12	97	BR1	151	OSC1_X2	205	WD13
44	MDC	98	BR2	152	VD33U0	206	WD14
45	MDIO	99	BR3	153	USBDM0	207	WD15
46	A0	100	BR4	154	USBDP0	208	VD33O
47	DABD1	101	BR5	155	GNDU0	209	OSC2_X1
48	DAAD2	102	BR6	156	USBREF0	210	OSC2_X2
49	VM	103	BR7	157	GND	211	GNDO
50	DABD2	104	BR8	158	VD33U1	212	GND
51	VREF	105	BR9	159	USBDM1	213	VC12
52	MD0	106	BR10	160	USBDP1	214	OUTVC12
53	MD1	107	CLBD	161	GNDU1	215	VD33R
54	MD2	108	WSBD	162	USBREF1	216	GNDR

4.2.3. Memory Config 3: SDRAM + NAND 16-bit Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	55	DRDQ3	109	**VD33**	163	**GND**
2	TEST	56	**GND**	110	VIN	164	CKOUT
3	STIN	57	**VC12**	111	**VA33**	165	NDCE0/
4	STOUT	58	**VM**	112	**AGND**	166	NDCE1/
5	MIDI_IN1	59	DRDQ4	113	SEL0	167	NDR|B/
6	MIDI_OUT1	60	DRDQ5	114	SEL1	168	NDALE
7	SPICK	61	DRDQ6	115	DABD1	169	NDCLE
8	SPICS0/	62	DRDQ7	116	REF_CLK	170	NDWE/
9	**VD33**	63	DRDQ8	117	CS/	171	NDRE/
10	TXD0	64	DRDQ9	118	RD/	172	**VD33**
11	TXD1	65	**VM**	119	WR/	173	**VD33**
12	RXD0	66	DRDQ10	120	IRQ	174	P5.8
13	RXD1	67	DRDQ11	121	A0	175	P5.9
14	TX_EN	68	DRDQ12	122	D0	176	P5.10
15	CRS_DV	69	DRDQ13	123	**VD33**	177	P5.11
16	RX_ER	70	DRDQ14	124	D1	178	DAAD5
17	ETH_RES/	71	DRDQ15	125	D2	179	DABD5
18	ROW0	72	**VM**	126	D3	180	DAAD4
19	ROW1	73	DRA4	127	D4	181	DABD4
20	ROW2	74	DRA5	128	D5	182	DAAD7
21	ROW3	75	DRA6	129	D6	183	DABD7
22	**VD33**	76	DRA7	130	D7	184	DAAD6
23	SPI0	77	DRA8	131	**VD12**	185	DABD6
24	SPI1	78	DRA9	132	MK8	186	DAAD3
25	SPI2	79	**VM**	133	MK9	187	**VD33**
26	SPI3	80	**VD12**	134	MK10	188	DAAD2
27	**VM**	81	DRA10	135	DABD0	189	DAAD1
28	DRCAS/	82	DRA11	136	DAAD0	190	P5.7
29	DRRAS/	83	DRA12	137	DABD2	191	NDIO0
30	DRWE/	84	DRA13	138	DABD3	192	NDIO1
31	DRCKE	85	DRBA0	139	**VD33**	193	NDIO2
32	DRCS0/	86	DRBA1	140	MDC	194	NDIO3
33	DRCS1/	87	**VM**	141	MDIO	195	NDIO4
34	**VM**	88	MK0	142	P6.5	196	NDIO5
35	DRCS2/	89	MK1	143	P6.6	197	NDIO6
36	DRCS3/	90	MK2	144	XWSBD1	198	NDIO7
37	DRA0	91	MK3	145	XCLBD1	199	NDIO8
38	DRA1	92	MK4	146	XWSBD0	200	**VD33**
39	DRA2	93	MK5	147	XCLBD0	201	NDIO9
40	DRA3	94	MK6	148	USBID	202	NDIO10
41	**VM**	95	MK7	149	FSOURCE	203	NDIO11
42	**VD12**	96	BR0	150	OSC1_X1	204	NDIO12
43	**VD12**	97	BR1	151	OSC1_X2	205	NDIO13
44	DRDS0	98	BR2	152	**VD33U0**	206	NDIO14
45	DRDS1	99	BR3	153	USBDM0	207	NDIO15
46	DRDM0	100	BR4	154	USBDP0	208	**VD33O**
47	DRDM1	101	BR5	155	**GNDU0**	209	OSC2_X1
48	DRCK/	102	BR6	156	USBREF0	210	OSC2_X2
49	**VM**	103	BR7	157	**GND**	211	**GNDO**
50	DRCK	104	BR8	158	**VD33U1**	212	**GND**
51	VREF	105	BR9	159	USBDM1	213	**VC12**
52	DRDQ0	106	BR10	160	USBDP1	214	**OUTVC12**
53	DRDQ1	107	CLBD	161	**GNDU1**	215	**VD33R**
54	DRDQ2	108	WSBD	162	USBREF1	216	**GNDR**

4.2.4. Memory Config 4: SDRAM + NAND 8-bit Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	55	DRDQ3	109	VD33	163	GND
2	TEST	56	GND	110	VIN	164	CKOUT
3	STIN	57	VC12	111	VA33	165	NDCE0/
4	STOUT	58	VM	112	AGND	166	NDCE1/
5	MIDI_IN1	59	DRDQ4	113	SEL0	167	NDR|B/
6	MIDI_OUT1	60	DRDQ5	114	SEL1	168	NDALE
7	SPICK	61	DRDQ6	115	DABD1	169	NDCLE
8	SPICS0/	62	DRDQ7	116	REF_CLK	170	NDWE/
9	VD33	63	DRDQ8	117	CS/	171	NDRE/
10	TXD0	64	DRDQ9	118	RD/	172	VD33
11	TXD1	65	VM	119	WR/	173	VD33
12	RXD0	66	DRDQ10	120	IRQ	174	P5.8
13	RXD1	67	DRDQ11	121	A0	175	P5.9
14	TX_EN	68	DRDQ12	122	D0	176	P5.10
15	CRS_DV	69	DRDQ13	123	VD33	177	P5.11
16	RX_ER	70	DRDQ14	124	D1	178	DAAD5
17	ETH_RES/	71	DRDQ15	125	D2	179	DABD5
18	ROW0	72	VM	126	D3	180	DAAD4
19	ROW1	73	DRA4	127	D4	181	DABD4
20	ROW2	74	DRA5	128	D5	182	DAAD7
21	ROW3	75	DRA6	129	D6	183	DABD7
22	VD33	76	DRA7	130	D7	184	DAAD6
23	SPI0	77	DRA8	131	VD12	185	DABD6
24	SPI1	78	DRA9	132	MK8	186	DAAD3
25	SPI2	79	VM	133	MK9	187	VD33
26	SPI3	80	VD12	134	MK10	188	DAAD2
27	VM	81	DRA10	135	DABD0	189	DAAD1
28	DRCAS/	82	DRA11	136	DAAD0	190	P5.7
29	DRRAS/	83	DRA12	137	DABD2	191	NDIO0
30	DRWE/	84	DRA13	138	DABD3	192	NDIO1
31	DRCKE	85	DRBA0	139	VD33	193	NDIO2
32	DRCS0/	86	DRBA1	140	MDC	194	NDIO3
33	DRCS1/	87	VM	141	MDIO	195	NDIO4
34	VM	88	MK0	142	P6.5	196	NDIO5
35	DRCS2/	89	MK1	143	P6.6	197	NDIO6
36	DRCS3/	90	MK2	144	XWSBD1	198	NDIO7
37	DRA0	91	MK3	145	XCLBD1	199	P4.8
38	DRA1	92	MK4	146	XWSBD0	200	VD33
39	DRA2	93	MK5	147	XCLBD0	201	P4.9
40	DRA3	94	MK6	148	USBID	202	P4.10
41	VM	95	MK7	149	FSOURCE	203	P4.11
42	VD12	96	BR0	150	OSC1_X1	204	P4.12
43	VD12	97	BR1	151	OSC1_X2	205	P4.13
44	DRDS0	98	BR2	152	VD33U0	206	P4.14
45	DRDS1	99	BR3	153	USBDM0	207	P4.15
46	DRDM0	100	BR4	154	USBDP0	208	VD33O
47	DRDM1	101	BR5	155	GNDU0	209	OSC2_X1
48	DRCK/	102	BR6	156	USBREF0	210	OSC2_X2
49	VM	103	BR7	157	GND	211	GNDO
50	DRCK	104	BR8	158	VD33U1	212	GND
51	VREF	105	BR9	159	USBDM1	213	VC12
52	DRDQ0	106	BR10	160	USBDP1	214	OUTVC12
53	DRDQ1	107	CLBD	161	GNDU1	215	VD33R
54	DRDQ2	108	WSBD	162	USBREF1	216	GNDR

4.3. Pin description

White cells describes Primary function of the pin
Grey cells describes Secondary function of the pin
Pink cells describes GPIO function of the pin
Yellow cells describes special function of the pin at start-up

PD indicates pin with built-in pull-down resistor. (PD) indicates that the pull-down can be disabled.
PU indicates pin with built-in pull-up resistor. (PU) indicates that the pull-down can be disabled.
5VT indicates a 5 volt tolerant Input or I/O pin.
MEM indicates a pad supplied by VM.
DR4, DR8, DR12 indicates driving capability at VOL, VOH (see § 7.3.- D.C. Characteristics)
SR3: If GPIO is used as input, an external 330Ω (min) serial resistor is needed for safe ROM boot.
SR7: If GPIO is used as input, an external 750Ω (min) serial resistor is needed for safe ROM boot.

4.3.1. Power Supply Group

Pin name	Pin#	Type	Mem Cfg	Description
VD12	42,43, 80,131	PWR	1-4	Power for the internal core, +1.2V nominal (1.2V ± 10 %). These pins must be connected to the output of the regulator OUTVC12 (pin 214). 100nF+10nF capacitors should be connected between each of these pins and a close ground plane. 10µF should be added on two opposite sides.
VC12	57,213	PWR	1-4	Power for the internal PLL and DLL, +1.2V nominal (1.2V ± 10 %). These pins must be connected to the output of the regulator OUTVC12 (pin 214). 10µF+100nF capacitors should be connected between these pins and a close ground pin (56, 211).
VD33	9,22,109, 123,139, 172,173, 187,200	PWR	1-4	+3.3V power for periphery. All these pins should be returned to nominal 3.3V. 100nF decoupling capacitors should be connected between half of these pins and ground plane
GND	56,157, 163,212	PWR	1-4	Digital ground. All these pins should be returned to a ground plane
GND	Exposed Pad	PWR	1-4	Digital ground, down bonded to the exposed pad (heatsink). For applications using DDR SDRAM, this pad must be connected to a ground plane during PCB layout. It can be left unconnected for other applications.
VD33O	208	PWR	1-4	+3.3V power for internal oscillator OSC2. A 100nF filtering capacitor should be connected between VD33O and GNDO.
GNDO	211	PWR	1-4	Digital ground for internal oscillator OSC2. This pin should be returned to the ground plane
VD33R	215	PWR	1-4	+3.3V power for internal 3.3V to 1.2 V regulator. A 10µF filtering capacitor should be connected between VD33R and GNDR.
GNDR	216	PWR	1-4	Digital ground for internal 3.3V to 1.2 V regulator. This pin should be returned to the ground plane
VD33U0, VD33U1	152,158	PWR	1-4	+3.3V power for internal USB ports. 10µF+100nF+10nF capacitors should be connected between VD33U0 and GNDU0, VD33U1 and GNDU1.
GNDU0, GNDU1	155,161	PWR	1-4	Digital ground for internal USB ports. These pins should be returned to a ground plane

Pin name	Pin#	Type	Mem Cfg	Description
VM	27,34,41, 49,58,65, 72,79,87	PWR	1-4	Memory PAD Power +2.25V to +3.6V. Depending on the memory type, all VM pins should be returned to 3.3V or 2.5V. 100nF capacitors should be connected between half of these pins and a close ground plane. 10nF capacitors should be connected between the other half of these pins and a close ground plane. 10µF should be added on both sides.
VA33	111	PWR	1-4	Analog power for the ADC. Should be connected to a clean analog +3.3V nominal. 10µF+100nF capacitors should be connected between VA33 and AGND.
AGND	112	PWR	1-4	Analog ground for ADC. Should be returned to a clean analog ground plane.
OUTVC12	214	PWR	1-4	3.3V to 1.2 V regulators output. The built-in regulator gives 1.2V for internal use. VC12 and VD12 pins should also be connected to this pin. Decoupling capacitors 3.3µF+100nF or 4.7µF+100nF must be connected between OUTVC12 pin and GNDR
FSOURCE	149	PWR	1-4	Fuse Program source input. - Left open or grounded (recommended) for normal operation. - Connected to +3.3V/12mA(min) power supply for fuse programming. 10µF+100nF capacitors should be connected between FSOURCE and ground plane.
VREF	51	In	1-4	VM/2 reference for memory pads MEM are in SSTL_2 mode (DDR). Grounded or not connected when memory pads MEM are in LVTTL mode (all functions, excepted DDR)

4.3.2. Test, Reset, Oscillators, USB, ADC, MIDI, Debug.

Pin name	Pin#	Type	Mem Cfg	Description
TEST	2	In PD	1-4	Test input. Should be grounded or left open.
RST/	1	In	1-4	Master reset. Schmitt trigger input. RST should be held low during at least 10ms after power is applied. On the rising edge of RST the chip enters its initialization routine.
OSC1_X1-OSC1_X2	150,151	-	1-4	Main Oscillator OSC1 - Dual crystal design: 12 MHz external crystal connection for USB embedded Ports and Ethernet controller. - Single crystal design: USB, Ethernet, System and audio clocks are derived fromOSC1. Crystal value can be: ° 12MHz if USB or Ethernet in use. ° 11.2896MHz or 12.288MHz if USB is not used - An external clock can be connected to OSC1_X1.
OSC2_X1-OSC2_X2	209,210	-	1-4	- Dual crystal design: System and audio clocks are derived from OSC2_X1-OSC2_X2. Crystal value can be 11.2896MHz or 12.288MHz. - Single crystal design: These pins should be left unconnected. - An external clock can be connected to OSC2_X1. (e.g., enslavement to external VCX0 driven by SAM5916B PWM generator)
USBDM0	153	I/O	1-4	USB D- connection (analog) of USB Port 0
USBDP0	154	I/O	1-4	USB D+ connection (analog) of USB Port 0
USBREF0	156	In	1-4	A 12kΩ ± 1% resistor should be connected between this pin and GNDU0. Unconnected if USB Port 0 is not used.
USBID	148	In 5VT	1-4	USB ID. Detect if A device or B device in case of USB Port 0 running in Dual Role mode.
MIDI_OUT2	148	Out DR4	1-4	Additional Serial MIDI Out.
P8.15	148	I/O 5VT DR4	1-4	General purpose I/O pin.
USBDM1	159	I/O	1-4	USB D- connection (analog) of USB Port 1
USBDP1	160	I/O	1-4	USB D+ connection (analog) of USB Port 1
USBREF1	162	In	1-4	A 12kΩ ± 1% resistor should be connected between this pin and GNDU1. Unconnected if USB Port 1 is not used.
VIN	110	In	1-4	Analog input of embedded ADC: Multiple sliders should be connected through external analog multiplexer like 4051. Channels should be selected by ROW0-ROW3.
MIDI_IN1	5	In 5VT (PU)	1-4	Serial MIDI In.
MIDI_IN2	5	In 5VT (PU)	1-4	Additional Serial MIDI In.
P0.14	5	I/O 5VT (PU) DR4	1-4	General purpose I/O pin.
MIDI_OUT1	6	Out DR4	1-4	Serial MIDI Out.
P0.9	6	I/O DR4	1-4	General purpose I/O pin.
STIN	3	In PD	1-4	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. It should be grounded or left open for normal operation.
STOUT	4	Out DR4	1-4	Serial test output. 57.6 kbauds async output used for firmware debugging.
MIDI_IN2	4	In (PU)	1-4	Additional Serial MIDI In.
P0.15	4	I/O (PU) DR4	1-4	General purpose I/O pin.

4.3.3. Multi-Purpose Quad SPI as primary function

Pin name	Pin#	Type	Mem Cfg	Description
SPICK	7	Out DR8	1-4	Data clock for Multi-purpose Quad SPI interface.
PWM_OUT	7	Out DR8	1-4	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.14	7	I/O DR8 SR3	1-4	General purpose I/O pin.
MC1	7	In	1-4	Memory Config 1. This pin is sensed at power-up. MC0-MC1 setting allows boot ROM code to start the right Memory Config.
SPICS0/	8	Out DR8[2]	1-4	Chip select 0 for Multi-purpose Quad SPI interface.
P7.15	8	I/O (PU) DR8 SR3	1-4	General purpose I/O pin.
SPI0	23	I/O DR12	1-4	SPI data 0. - Serial Output to SI peripheral Input for Single bit data commands (MOSI). - Serial IO0 for Quad commands.
SPDIF_OUT	23	Out DR12	1-4	SPDIF output.
P7.10	23	I/O DR12 SR3	1-4	General purpose I/O pin.
SPI1	24	I/O DR4	1-4	SPI data 1. - Serial Input from SO peripheral Output for Single bit data commands (MISO). - Serial IO1 for or Quad commands.
SPDIF_IN	24	In	1-4	SPDIF input.
P7.11	24	I/O DR4	1-4	General purpose I/O pin.
SPI2	25	I/O DR4	1-4	SPI data 2. Serial IO2 Quad commands
PWM_OUT	25	Out DR4	1-4	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.12	25	I/O (PU) DR4	1-4	General purpose I/O pin.
SPI3	26	I/O DR4	1-4	SPI data 2. Serial IO2 Quad commands
SPDIF_IN	26	In (PU) DR4	1-4	SPDIF input
P7.13	26	I/O (PU) DR4	1-4	General purpose I/O pin.

4.3.4. Ethernet as primary function

Pin name	Pin#	Type	Mem Cfg	Description
REF_CLK	116	Out DR12	1-4	25MHz RMII reference clock to the Ethernet PHY.
SPICS1/	116	Out DR12	1-4	Chip select 1 for Multi-purpose Quad SPI interface.
P8.0	116	I/O (PU) DR12	1-4	General purpose I/O pin.
ETH_RES/	17	Out DR4	1-4	Reset output to the Ethernet PHY
XWSBD1	17	In	1-4	External word select clock for digital audio inputs DAAD[7:0].
P8.1	17	I/O DR4	1-4	General purpose I/O pin.
RX_ER	16	In	1-4	RMII Receive Error from the Ethernet PHY.
XCLBD1	16	In	1-4	External clock bit for digital audio inputs DAAD[7:0].
P8.2_IntB	16	I/O DR4	1-4	General purpose I/O pin. External Interrupt source IntB.
RXD0	12	In	1-4	RMII Receive Data 0 from the Ethernet PHY.
DAAD6	12	In	1-4	Stereo audio digital input 6, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.3	12	I/O DR4	1-4	General purpose I/O pin.
RXD1	13	In	1-4	RMII Receive Data 1 from the Ethernet PHY.
DAAD7	13	In	1-4	Stereo audio digital input 7, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.4	13	I/O DR4	1-4	General purpose I/O pin.
CRS_DV	15	In	1-4	RMII Carrier Sense/Receive Data Valid from the Ethernet PHY
DABD6	15	Out DR4	1-4	Stereo audio digital output 6, I2S or MSB format.
P8.5	15	I/O DR4	1-4	General purpose I/O pin.
TXD0	10	Out DR4	1-4	RMII Transmit Data 0 to the Ethernet PHY.
DABD7	10	Out DR4	1-4	Stereo audio digital output 7, I2S or MSB format.
P8.6	10	I/O DR4	1-4	General purpose I/O pin.
TXD1	11	Out DR4	1-4	RMII Transmit Data 1 to the Ethernet PHY.
SPICS2/	11	Out DR4	1-4	Chip select 2 for Multi-purpose Quad SPI interface.
P8.7	11	I/O (PU) DR4	1-4	General purpose I/O pin.
TX_EN	14	Out DR4	1-4	RMII Transmit Enable to the Ethernet PHY.
SPICS3/	14	Out DR4	1-4	Chip select 3 for Multi-purpose Quad SPI interface.
P8.8	14	I/O (PU) DR4	1-4	General purpose I/O pin.
MDC	44	Out MEM	2	Management Interface (MII) Clock to the Ethernet PHY.
XWSBD0	44	In MEM	2	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
P8.9	44	I/O MEM	2	General purpose I/O pin.
MDIO	45	I/O MEM	2	Management Interface (MII) Data I/O to the Ethernet PHY.
XCLBD0	45	In MEM	2	External clock bit for digital audio inputs DAAD[7:0].
P8.10	45	I/O MEM	2	General purpose I/O pin.
MDC	140	Out DR4	3,4	Management Interface (MII) Clock to the Ethernet PHY.
XWSBD0	140	In	3,4	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
P8.9	140	I/O DR4	3,4	General purpose I/O pin.
MDIO	141	I/O DR4	3,4	Management Interface (MII) Data I/O to the Ethernet PHY.
XCLBD0	141	In	3,4	External clock bit 0 for digital audio inputs DAAD[7:0].
P8.10	141	I/O DR4	3,4	General purpose I/O pin.

4.3.5. Host Parallel Interface as primary function

Pin name	Pin#	Type	Mem Cfg	Description
D0-D7	122, 124-130	I/O 5VT DR8	1-4	Host parallel interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0-A1 address input.
DAAD2	122	In 5VT	1-4	Stereo audio digital input 2, I2S or MSB format.
DABD4	124	Out DR8	1-4	Stereo audio digital output 4, I2S or MSB format.
DABD3	125	Out DR8	1-4	Stereo audio digital output 3, I2S or MSB format.
DABD2	126	Out DR8	1-4	Stereo audio digital output 2, I2S or MSB format.
XWSBD1	127	In 5VT	1-4	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD1	128	In 5VT	1-4	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD0	129	In 5VT	1-4	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
XCLBD0	130	In 5VT	1-4	External clock bit 0 for digital audio inputs DAAD[7:0].
P0.0-P0.7	122, 124-130	I/O 5VT DR8	1-4	General purpose I/O pins. Can be individually programmed as input or output.
IRQ	120	Out DR12	1,3,4	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	120	Out DR12	1,3,4	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8_IntA	120	I/O DR12	1,3,4	General purpose I/O pin. External Interrupt source IntA.
A0	121	In 5VT	1,3,4	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	121	In 5VT	1,3,4	Serial Slave Synchronous Interface clock input.
P0.10	121	I/O 5VT DR8	1,3,4	General purpose I/O pin.
CS/	117	In 5VT	1,3,4	Host parallel interface chip select, active low.
SSYNC	117	In 5VT	1,3,4	Serial Slave Synchronous Interface input sync signal.
P0.11	117	I/O 5VT DR8	1,3,4	General purpose I/O pin.
WR/	119	In 5VT	1,3,4	Host parallel interface write, active low. D7-D0 or D15-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	119	In 5VT	1,3,4	Serial Slave Synchronous Interface input data.
P0.12	119	I/O 5VT DR8	1,3,4	General purpose I/O pin.
RD/	118	In 5VT	1,3,4	Host parallel interface read, active low. D7-D0 or D15-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	118	Out 5VT DR8	1,3,4	Additional Serial MIDI Out. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	118	I/O 5VT DR8	1,3,4	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot.** **If used as input, should not be driven low by external device while ROM boot.**
A0	46	Out MEM	2	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	46	In MEM	2	Serial Slave Synchronous Interface clock input.
P0.10	46	I/O MEM	2	General purpose I/O pin.

Pin name	Pin#	Type	Mem Cfg	Description
IRQ	31	Out MEM	2	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	31	Out MEM	2	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8	31	I/O MEM	2	General purpose I/O pin. External Interrupt source INTA
CS/	28	In MEM	2	Host parallel interface chip select, active low.
SSYNC	28	In MEM	2	Serial Slave Synchronous Interface input sync signal.
P0.11	28	I/O MEM	2	General purpose I/O pin.
WR/	30	In MEM	2	Host parallel interface write, active low. D7-D0 or D15-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	30	In MEM	2	Serial Slave Synchronous Interface input data.
P0.12	30	I/O MEM	2	General purpose I/O pin.
RD/	29	In MEM	2	Host parallel interface read, active low. D7-D0 or D15-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	29	Out MEM	2	Additional Serial MIDI Out. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	29	I/O MEM	2	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot.** **If used as input, should not be driven low by external device while ROM boot.**

4.3.6. Versatile IOs as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MK0-MK10	88-95, 132-134	I/O 5VT DR8	1-4	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: Second Kbd contact / switch status. When SEL0=1 then MK[0-10] holds the keyboard key-on or second contact status. When SEL0=0 then MK[0-10] gives the switch status from ROW[0-3].
D8-D15	88-95	I/O 5VT DR8	1-4	Host parallel interface upper data bits when pin A1 = 1 (mode 1)
A1	132	In 5VT	1-4	Host parallel interface address 1: A1=0 selects mode 0 for communication/control A1=1 selects mode 1 for fast 8/16bit data transfer
XFR_RDY	133	Out DR8	1-4	Host parallel interface “Transfer Ready” output. When A1 = 1, this pin is reflecting status of current data read/write. Before beginning next read/write, host has to check XFR_RDY is 1
DAAD0	134	In 5VT	1-4	Stereo audio digital input 0, I2S or MSB format.
BR0-BR10	96-106	I/O 5VT DR8	1-4	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: First Kbd contact / Led data. When SEL0=1 then BR[0-10] holds the keyboard key-off or first contact status. When SEL0=0 then BR[0-10] holds the led data from ROW[0-3].
DAAD7	96	In 5VT	1-4	Stereo audio digital input 7, I2S or MSB format.
DABD7	97	Out DR8	1-4	Stereo audio digital output 7, I2S or MSB format.
DAAD6	98	In 5VT	1-4	Stereo audio digital input 6, I2S or MSB format.
DABD6	99	Out DR8	1-4	Stereo audio digital output 6, I2S or MSB format.
DABD3	100	Out DR8	1-4	Stereo audio digital output 3, I2S or MSB format.
DAAD2	101	In 5VT	1-4	Stereo audio digital input 2, I2S or MSB format.
DAAD1	102	In 5VT	1-4	Stereo audio digital input 1, I2S or MSB format.
XCLBD1	103	In 5VT	1-4	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD1	104	In 5VT	1-4	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD0	105	In 5VT	1-4	External clock bit 0 for digital audio inputs DAAD[7:0].
XWSBD0	106	In 5VT	1-4	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
ROW0-ROW3	18-21	I/O 5VT DR8	1-4	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: ROW signals select keyboard, switches/Leds row and external slider analog multiplexer (4051) channel. Sixteen rows combined with eleven BR/MK columns allow to control 176 keys, 176 switches, 88 Leds and 16 sliders.
DAAD5	18	In 5VT	1-4	Stereo audio digital input 5, I2S or MSB format.
DABD4	19	Out DR8	1-4	Stereo audio digital output 4, I2S or MSB format.
DABD5	20	Out DR8	1-4	Stereo audio digital output 5, I2S or MSB format.
DAAD4	21	In 5VT	1-4	Stereo audio digital input 4, I2S or MSB format.
SEL0-SEL1	113-114	I/O 5VT DR8	1-4	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: If SEL0=1, BR[0-10] & MK[0-10] hold keyboard contact input data. If SEL0=0 MK[0-10] holds switch status input, BR[0-10] holds led data output. Sel1 can be used in case of kbd, with other matrix than 8*11, multiple kbd or kbd with 3 switches per key.
DAAD3	113	In 5VT	1-4	Stereo audio digital input 3, I2S or MSB format.
DABD0	114	Out DR8	1-4	Stereo audio digital output 0, I2S or MSB format.

4.3.7. SDR / DDR as primary function

Pin name	Pin#	Type	Mem Cfg	Description
DRCAS/	28	Out MEM	1,3,4	Column address strobe for external SDR SDRAM or DDR SDRAM memory.
DRRAS/	29	Out MEM	1,3,4	Row address strobe for external SDR SDRAM or DDR SDRAM memory.
DRWE/	30	Out MEM	1,3,4	Write enable for external SDR SDRAM or DDR SDRAM memory.
DRCKE	31	Out MEM	1,3,4	Clock Enable for external SDR SDRAM or DDR SDRAM memory.
DRDM0, DRDM1	46,47	Out MEM	1,3,4	Input/output mask for external SDR SDRAM or DDR SDRAM.
DRCK	50	Out MEM	1,3,4	Positive clock for external SDR SDRAM or DDR SDRAM memory.
DRCS0/	32	Out MEM	1,3,4	Chip select 0 for external DDR SDRAM memory.
SPICS1/	32	Out MEM	1,3,4	Chip select 1 for Multi-purpose Quad SPI interface..
P3.4	32	I/O MEM SR7	1,3,4	General purpose I/O pin.
DRCS1/	33	Out MEM	1,3,4	Chip select 1 for external DDR SDRAM memory.
XIO/_DBGCS/	33	Out MEM	1	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM. **External 100k pull-up resistor is needed for safe ROM boot.**
P3.5	33	I/O MEM SR7	1,3,4	General purpose I/O pin.
DRCS2/	35	Out MEM	1,3,4	Chip select 2 for external DDR SDRAM memory.
SPICS2/	35	Out MEM	1,3,4	Chip select 2 for Multi-purpose Quad SPI interface..
P3.6	35	I/O MEM SR7	1,3,4	General purpose I/O pin..
DRCS3/	36	Out MEM	1,3,4	Chip select 3 for external DDR SDRAM memory.
XIO/_DBGCS/	36	Out MEM	1	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM. **External 100k pull-up resistor is needed for safe ROM boot.**
P3.7	36	I/O MEM SR7	1-4	General purpose I/O pin.
DRA0-DRA13	37-40, 73-78, 81-84	Out MEM	1,3,4	Address for external DDR SDRAM memory.
P10.0-P10.13	37-40, 73-78, 81-84	I/O MEM	1,3,4	General purpose I/O pin.
DRBA0,DRBA1	85,86	Out MEM	1,3,4	Bank address for external DDR SDRAM memory.
P10.14-P10.15	85,86	I/O MEM	1,3,4	General purpose I/O pin.
DRDQ0-DRDQ15	52-55, 59-64, 66-71	I/O MEM	1,3,4	Data for external DDR SDRAM memory.
P9.0-P9.15	52-55, 59-64, 66-71	I/O MEM	1,3,4	General purpose I/O pin.
DRCK/	48	Out MEM	1,3,4	Negative clock for external DDR SDRAM memory.
DAAD2	48	Out MEM	1,3,4	Stereo audio digital input 2, I2S or MSB format.
P3.8	48	I/O MEM	1,3,4	General purpose I/O pin.
DRDS0,DRDS1	44,45	I/O MEM	1,3,4	Data Strobe for external DDR SDRAM memory.
MDC	44	Out MEM	1,3,4	Management Interface (MII) Clock to the Ethernet PHY.
MDIO	45	I/O MEM	1,3,4	Management Interface (MII) Data I/O to the Ethernet PHY.
P3.9	44	I/O MEM	1,3,4	General purpose I/O pin.
P3.10	45	I/O MEM	1,3,4	General purpose I/O pin.

4.3.8. SRAM as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MA0-MA15	37-40, 73-78, 81-86	Out MEM	2	Address bits for external SRAM memory, up to 1Mbit (64kx16).
P10.0-P10.15	37-40, 73-78, 81-86	I/O MEM	2	General purpose I/O pin.
MA16-MA18	117-119	Out DR8	2	Address bits for external SRAM memory, extension to 8Mbits (512kx16).
P1.0-P1.2	117-119	I/O 5VT (PD) DR8	2	General purpose I/O pin.
MD0-MD15	52-55, 59-64, 66-71	I/O MEM	2	Data bus for external SRAM memory.
P9.0-P9.15	52-55, 59-64, 66-71	I/O MEM	2	General purpose I/O pin.
MWE/	120	Out DR12	2	External SRAM memory write enable, active low.
P1.11	120	I/O (PU) DR12	2	General purpose I/O pin.
MOE/	121	Out DR8	2	External SRAM memory output enable, active low.
P1.12	121	I/O 5VT (PU) DR8	2	General purpose I/O pin.
SRCS/	115	Out DR4	2	External SRAM memory chip select, active low.
P1.15	115	I/O (PU) DR4	2	General purpose I/O pin.

4.3.9. NOR Flash as primary function

Pin name	Pin#	Type	Mem Cfg	Description
WA0	182	Out DR12	1,2	Address bits for external NOR Flash memory, up to 2Gbit (256MByte).
WA1-WA7	183-186, 188-190	Out DR8		
WA8-WA15	174-181,	Out DR4		
WA16-WA18	167-169,	Out DR8		
WA19-WA26	140-147	Out DR4		
P5.0	182	I/O 5VT DR12 SR3	1,2	General purpose I/O pin.
P5.1-P5.6	183-186, 188-189	I/O 5VT DR8 SR3	1,2	General purpose I/O pin.
P5.7	190,	I/O 5VT DR8 SR3	1-4	General purpose I/O pin.
P5.8-P5.11	174-177,	I/O DR4 SR3	1-4	General purpose I/O pin.
P5.12-P5.15	178-181,	I/O DR4 SR3	1,2	General purpose I/O pin.
P6.0-P6.2	167-169	I/O 5VT (PD) DR8 SR3	1,2	General purpose I/O pin.
P6.3-P6.4	140-141	I/O (PD) DR4 SR3	1,2	General purpose I/O pin.
P6.5,P6.6	142-143	I/O (PD) DR4 SR3	1,2,3	General purpose I/O pin.
P6.7-P6.9	144-146	I/O (PD) DR4 SR3	1,2	General purpose I/O pin.
P6.10_IntC	147	I/O (PD) DR4 SR3	1,2	General purpose I/O pin. External interrupt source IntC.
WWE/	170	Out DR8	1,2	External NOR Flash memory write enable, active low.
P6.11	170	I/O 5VT (PU) DR8 SR3	1,2	General purpose I/O pin.
WOE/	171	Out DR4	1,2	External NOR Flash memory output enable, active low.
P6.12	171	I/O (PU) DR4 SR3	1,2	General purpose I/O pin.
NRCS10/	135	Out DR12	1,2	External NOR Flash memory chip select 0, active low.
P6.13	135	I/O (PU) DR12 SR3	1,2	General purpose I/O pin.
NRCS11/	136	Out DR4	1,2	External NOR Flash memory chip select 1, active low.
P6.14	136	I/O (PU) DR4	1,2	General purpose I/O pin.
NRCS12/	137	Out DR4	1,2	External NOR Flash memory chip select 2, active low.
P6.15	137	I/O (PU) DR4	1,2	General purpose I/O pin.
NRCS13/	138	Out DR4	1,2	External NOR Flash memory chip select 3, active low. **External 100k pull-up resistor is needed for safe ROM boot.**
WA27	138	Out DR4	1,2	Address bit for external NOR Flash memory, extension to 4Gbit (512MByte). **External 100k pull-down resistor is needed for safe ROM boot.**
P3.11	138	I/O DR4	1,2	General purpose I/O pin.
WD0-WD6	191-197	I/O DR8	1,2	Data bus for external NOR Flash memory.
WD7-WD15	198-199, 201-207	I/O DR4		
P4.0-P4.6	191-197	I/O 5VT DR8	1,2	General purpose I/O pin.
P4.7-P4.15	198-199, 201-207	I/O DR4	1,2	General purpose I/O pin.

4.3.10. NAND Flash as primary function

Pin name	Pin#	Type	Mem Cfg	Description
NDIO0-NDIO6	191-197	I/O DR8	3,4	Data bus for external 8-bit NAND Flash memory.
NDIO7	198	I/O DR4		
NDCE0/	165	Out DR12	3,4	External NAND Flash memory chip select 0, active low
NDCE1/	166	Out DR4	3,4	External NAND Flash memory chip select 1, active low
P3.12	166	I/O (PU) DR4	3,4	General purpose I/O pin.
NDR|B/	167	In 5VT	3,4	External NAND Flash Ready Busy/ status. Indicates target array activity. External pull-up resistor is needed if NAND Flash R|B/ is open-drain output.
NDALE	168	Out DR8	3,4	External NAND Flash Address Latch Enable. Load an address from I/O[7:0] into the address register.
NDCLE	169	Out DR8	3,4	External NAND Flash Command Latch Enable. Load a command from I/O[7:0] into the command register
NDWE/	170	Out DR8	3,4	External NAND Flash Write Enable. Transfer commands, address, and serial data from SAM5916B to the NAND Flash.
NDRE/	171	Out DR4	3,4	External NAND Flash Read Enable. Transfer serial data from the NAND Flash to SAM5916B.
NDIO8-NDIO15	199, 201-207	I/O DR4	4	Data bus extension for external 16-bit NAND Flash memory.
P4.8-P4.15	199, 201-207	I/O DR4 SR3	3,4	General purpose I/O pin.

4.3.11. Digital Audio as primary function

Pin name	Pin#	Type	Mem Cfg	Description
CKOUT	164	Out DR4	1-4	Audio master clock for external DAC and ADC. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, 768xFs, Fs being the DAC and ADC sampling rate.
MC0	164	In	1-4	Memory Config 0. This pin is sensed at power up. MC1|MC0 setting allows boot ROM code to start the right Memory Config.
CLBD	107	Out DR4	1-4	Audio bit clock for DABD0-DABD7 and for DAAD0-DAAD7.
FS1	107	In	1-4	Freq. Sense 1, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq on oscillator OSC1 as follow: 00->12MHz 01->9.6MHz, 10->11.2896MHz, 11->12.288MHz
WSBD	108	I/O DR4	1-4	Out by default: Audio left/right channel select for DABD0-DABD7 and for DAAD0-DAAD7. In: WSBD from external master audio device for full audio sync without external VCXO. Same Master clock is needed on SAM5916B and external master device.
FS0	108	In	1-4	Freq. Sense 0, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq on oscillator OSC1 (see FS1).
DAAD0	166	In (PD)	1,2	Stereo audio digital input 0, I2S or MSB format.
SPDIF_IN	166	In (PD)	1,2	SPDIF input.
P2.0	166	I/O (PD) DR4	1,2	General purpose I/O pin.
DAAD0	136	In (PD)	3,4	Stereo audio digital input 0, I2S or MSB format.
SPDIF_IN	136	In (PD)	3,4	SPDIF input.
P2.0	136	I/O (PD) DR4	3,4	General purpose I/O pin.

Pin name	Pin#	Type	Mem Cfg	Description
DAAD1	33	In MEM (PD)	2	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	33	Out MEM	2	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	33	I/O MEM (PD)	2	General purpose I/O pin.
DAAD1	189	In 5VT (PD)	3,4	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	189	Out DR8	3,4	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	189	I/O 5VT (PD) DR8	3,4	General purpose I/O pin.
DAAD2	48	In MEM (PD)	2	Stereo audio digital input 2, I2S or MSB format.
MIDI_OUT2	48	Out MEM	2	Additional Serial MIDI Out.
P2.2	48	I/O MEM (PD)	2	General purpose I/O pin.
DAAD2	188	In 5VT (PD)	3,4	Stereo audio digital input 2, I2S or MSB format.
MIDI_OUT2	188	Out DR8	3,4	Additional Serial MIDI Out.
P2.2	188	I/O 5VT (PD) DR8	3,4	General purpose I/O pin.
DAAD3	35	In MEM (PD)	2	Stereo audio digital input 3, I2S or MSB format.
P2.3	35	I/O MEM (PD)	2	General purpose I/O pin.
DAAD3	186	In 5VT (PD)	3,4	Stereo audio digital input 3, I2S or MSB format.
P2.3	186	I/O 5VT (PD) DR8	3,4	General purpose I/O pin.
DAAD4	180	In (PD)	3,4	Stereo audio digital input 4, I2S or MSB format.
P2.4	180	I/O (PD) DR4	3,4	General purpose I/O pin.
DAAD5	178	In (PD)	3,4	Stereo audio digital input 5, I2S or MSB format.
P2.5	178	I/O (PD) DR4	3,4	General purpose I/O pin.
DAAD6	184	In 5VT (PD)	3,4	Stereo audio digital input 6, I2S or MSB format.
P2.6	184	I/O 5VT (PD) DR8	3,4	General purpose I/O pin.
DAAD7	182	In 5VT (PD)	3,4	Stereo audio digital input 7, I2S or MSB format.
P2.7	182	I/O 5VT (PD) DR12	3,4	General purpose I/O pin.
DABD0	165	Out DR12	1,2	Stereo audio digital output 0, I2S or MSB format.
SPDIF_OUT	165	Out DR12	1,2	SPDIF output.
P2.15	165	I/O DR12	1,2	General purpose I/O pin.
DABD0	135	Out DR12	3,4	Stereo audio digital output 0, I2S or MSB format.
SPDIF_OUT	135	Out DR12	3,4	SPDIF output.
P2.15	135	I/O DR12	3,4	General purpose I/O pin.
DABD1	115	Out DR4	1,3,4	Stereo audio digital output 1, I2S or MSB format.
XIO/_DBGCS/	115	Out DR4	1	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM.
P2.8	115	I/O (PU) DR4	1,3,4	General purpose I/O pin.
DABD1	47	Out MEM	2	Stereo audio digital output 1, I2S or MSB format.
XIO/_DBGCS/	47	Out MEM	2	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM. **External 100k pull-up resistor is needed for safe ROM boot.**
P2.8	47	I/O MEM	2	General purpose I/O pin.
DABD2	50	Out MEM	2	Stereo audio digital output 2, I2S or MSB format.
P2.9	50	I/O MEM	2	General purpose I/O pin.
DABD2	137	Out DR4	3,4	Stereo audio digital output 2, I2S or MSB format.
P2.9	137	I/O DR4	3,4	General purpose I/O pin.

Pin name	Pin#	Type	Mem Cfg	Description
DABD3	32	Out MEM	2	Stereo audio digital output 3, I2S or MSB format.
P2.10	32	I/O MEM	2	General purpose I/O pin.
DABD3	138	Out DR4	3,4	Stereo audio digital output 3, I2S or MSB format.
P2.10	138	I/O DR4	3,4	General purpose I/O pin.
DABD4	181	Out DR4	3,4	Stereo audio digital output 4, I2S or MSB format.
P2.11	181	I/O DR4	3,4	General purpose I/O pin.
DABD5	179	Out DR4	3,4	Stereo audio digital output 5, I2S or MSB format.
P2.12	179	I/O DR4	3,4	General purpose I/O pin.
DABD6	185	Out DR8	3,4	Stereo audio digital output 6, I2S or MSB format.
P2.13	185	I/O 5VT DR8	3,4	General purpose I/O pin.
DABD7	183	Out DR8	3,4	Stereo audio digital output 7, I2S or MSB format.
P2.14	183	I/O 5VT DR8	3,4	General purpose I/O pin.
XWSBD1	144	In (PD)	3,4	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
P3.0	144	I/O (PD) DR4	3,4	General purpose I/O pin.
XCLBD1	145	In (PD)	3,4	External clock bit 1 for digital audio inputs DAAD[7:0].
P3.1	145	I/O (PD) DR4	3,4	General purpose I/O pin.
XWSBD0	146	In (PD)	3,4	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
P3.2	146	I/O (PD) DR4	3,4	General purpose I/O pin.
XCLBD0	147	In (PD)	3,4	External clock bit for digital audio inputs DAAD[7:0].
P3.3	147	I/O (PD) DR4	3,4	General purpose I/O pin.

4.4. Primary & Secondary functions quick view

4.4.1. Key table

Function Code	Function description	Available in…
1	Multi-purpose Quad SPI interface	Mem. Config. 1-4
2	Ethernet MAC	Mem. Config. 1-4
3	Host Parallel Interface (8-bit)	Mem. Config. 1-4
4	Host Parallel Interface 16-bit extension	Mem. Config. 1-4
5	UART / MIDI interface	Mem. Config. 1-4
6	Debug interface	Mem. Config. 1-4
7	Serial Slave Synchronous interface	Mem. Config. 1-4
8	I2S Digital Audio Interface	Mem. Config. 1-4 (see Note1)
9	SPDIF Digital Audio Interface	Mem. Config. 1-4
10	Versatile IOs (VIO)	Mem. Config. 1-4
11	DDR & SDR SDRAM controller on Memory Port 0	Mem. Config. 1, 3, 4
12	DDR SDRAM extension on Memory Port 0	Mem. Config. 1, 3, 4
13	SRAM Controller on Memory Port 0	Mem. Config. 2
14	NOR Flash Controller on Memory Port 1	Mem. Config. 1, 2
15	NAND Flash Controller on Memory Port 1	Mem. Config. 3, 4
16	NAND Flash 16-bit extension	Mem. Config. 3
17	USB High Speed Host, Device or Dual-Role Port 0	Mem. Config. 1-4
18	USB High Speed Host only, Port 1	Mem. Config. 1-4

Note1: All Digital Audio Signals are not available for each Memory Configuration.

4.4.2. Functions per pin

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	TST				Config 1-4
	RST/				Config 1-4
	OSC2_X1-OSC2_X2				Config 1-4
	VIN				Config 1-4
5	MIDI_OUT1 (UART Tx)			P0,9	Config 1-4
5	MIDI_IN1 (UART Rx)	5	MIDI_IN2	P0.14	Config 1-4
6	STIN				Config 1-4
6	STOUT	5	MIDI_IN2	P0.15	Config 1-4
	Quad SPI				
1	SPICK		PWM_OUT	P7.14	Config 1-4
1	SPICS0/			P7.15	Config 1-4
1	SPI0 (MOSI)	9	SPDIF_OUT	P7.10	Config 1-4
1	SPI1 (MISO)	9	SPDIF_IN	P7.11	Config 1-4
1	SPI2		PWM_OUT	P7.12	Config 1-4
1	SPI3	9	SPDIF_IN	P7.13	Config 1-4
	Ethernet				
2	REF_CLK	1	SPICS1/	P8.0	Config 1-4
2	ETH_RES/	8	XWSBD1	P8.1	Config 1-4
2	RX_ER	8	XCLBD1	P8.2/INTB	Config 1-4
2	RXD0	8	DAAD6	P8.3	Config 1-4
2	RXD1	8	DAAD7	P8.4	Config 1-4
2	CRS_DV	8	DABD6	P8.5	Config 1-4
2	TXD0	8	DABD7	P8.6	Config 1-4
2	TXD1	1	SPICS2/	P8.7	Config 1-4
2	TX_EN	1	SPICS3/	P8.8	Config 1-4
2	MDC	8	XWSBD0	P8.9	Config 2, 3, 4
2	MDIO	8	XCLBD0	P8.10	Config 2, 3, 4
	Host Parallel Interface				
3	D0	8	DAAD2	P0.0	Config 1-4
3	D1	8	DABD4	P0.1	Config 1-4
3	D2	8	DABD3	P0.2	Config 1-4
3	D3	8	DABD2	P0.3	Config 1-4
3	D4	8	XWSBD1	P0.4	Config 1-4
3	D5	8	XCLBD1	P0.5	Config 1-4
3	D6	8	XWSBD0	P0.6	Config 1-4
3	D7	8	XCLBD0	P0.7	Config 1-4
3	IRQ	7	SSINT/	P0.8/INTA	Config 1-4
3	A0	7	SSCLK	P0.10	Config 1-4
3	CS/	7	SSYNC	P0.11	Config 1-4
3	WR/	7	SSDIN	P0.12	Config 1-4
3	RD/	5	MIDI_OUT2	P0.13	Config 1-4

(To be continued)

(Continued)

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	Versatile IOs				
9	MK0-MK7	4	D8-D15		Config 1-4
9	MK8	4	A1		Config 1-4
9	MK9	4	XFR_RDY		Config 1-4
9	MK10	8	DAAD0		Config 1-4
9	BR0	8	DAAD7		Config 1-4
9	BR1	8	DABD7		Config 1-4
9	BR2	8	DAAD6		Config 1-4
9	BR3	8	DABD6		Config 1-4
9	BR4	8	DABD3		Config 1-4
9	BR5	8	DAAD2		Config 1-4
9	BR6	8	DAAD1		Config 1-4
9	BR7	8	XCLBD1		Config 1-4
9	BR8	8	XWSBD1		Config 1-4
9	BR9	8	XCLBD0		Config 1-4
9	BR10	8	XWSBD0		Config 1-4
9	ROW0	8	DAAD5		Config 1-4
9	ROW1	8	DABD4		Config 1-4
9	ROW2	8	DABD5		Config 1-4
9	ROW3	8	DAAD4		Config 1-4
9	SEL0	8	DAAD3		Config 1-4
9	SEL1	8	DABD0		Config 1-4
	SDR / DDR				
11	DRCAS/				Config 1, 3, 4
11	DRRAS/				Config 1, 3, 4
11	DRWE/				Config 1, 3, 4
11	DRCKE				Config 1, 3, 4
11	DRDM0				Config 1, 3, 4
11	DRDM1				Config 1, 3, 4
11	DRCK				Config 1, 3, 4
11	DRCS0/	1	SPICS1/	P3.4	Config 1, 3, 4
11	DRCS1/		XIO/_DBGCS/	P3.5	Config 1, 3, 4
11	DRCS2/	1	SPICS2/	P3.6	Config 1, 3, 4
11	DRCS3/		XIO/_DBGCS/	P3.7	Config 1, 3, 4
11	DRA0-DRA13			P10.0-P10.13	Config 1, 3, 4
11	DRBA0,DRBA1			P10.14,P10.15	Config 1, 3, 4
11	DRDQ0-DRDQ15			P9.0-P9.15	Config 1, 3, 4
12	DRCK/	8	DAAD2	P3.8	Config 1, 3, 4
12	DRDS0	2	MDC	P3.9	Config 1, 3, 4
12	DRDS1	2	MDIO	P3.10	Config 1, 3, 4
	SRAM				
13	MA0-MA15			P10.0-P10.15	Config 2
13	MA16-MA18			P1.0-P1.2	Config 2
13	MD0-MD15			P9.0-P9.15	Config 2
13	MWE/			P1.11	Config 2
13	MOE/			P1.12	Config 2
13	SRCS/			P1,15	Config 2

(To be continued)

(Continued)

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	NOR Flash				
14	WA0-WA15			P5.0-P5.15	Config 1, 2
14	WA16-WA25			P6.0-P6.9	Config 1, 2
14	WA26			P6.10/INTC	Config 1, 2
14	WWE/			P6.11	Config 1, 2
14	WOE/			P6.12	Config 1, 2
14	NRCS10/			P6.13	Config 1, 2
14	NRCS11/			P6.14	Config 1, 2
14	NRCS12/			P6.15	Config 1, 2
14	NRCS13/	14	WA27	P3.11	Config 1, 2
14	WD0-WD15			P4.0-P4.15	Config 1, 2
	NAND Flash				
15	NDIO0-NDIO7				Config 3, 4
15	NDCE0/				Config 3, 4
15	NDCE1/			P3,12	Config 3, 4
15	NDR|B/				Config 3, 4
15	NDALE				Config 3, 4
15	NDCLE				Config 3, 4
15	NDWE/				Config 3, 4
15	NDRE/				Config 3, 4
16	NDIO8-NDIO15			P4.8-P4.15	Config 3
	Digital Audio				
8	CKOUT				Config 1-4
8	WSBD				Config 1-4
8	CLBD				Config 1-4
8	DAAD0	9	SPDIF_IN	P2.0	Config 1-4
8	DAAD1		PWM_OUT	P2.1	Config 2, 3, 4
8	DAAD2	5	MIDI_OUT2	P2.2	Config 2, 3, 4
8	DAAD3			P2.3	Config 2, 3, 4
8	DAAD4			P2.4	Config 3, 4
8	DAAD5			P2.5	Config 3, 4
8	DAAD6			P2.6	Config 3, 4
8	DAAD7			P2.7	Config 3, 4
8	DABD0	9	SPDIF_OUT	P2,15	Config 1-4
8	DABD1		XIO/_DBGCS/	P2.8	Config 1-4
8	DABD2			P2.9	Config 2, 3, 4
8	DABD3			P2.10	Config 2, 3, 4
8	DABD4			P2.11	Config 3, 4
8	DABD5			P2.12	Config 3, 4
8	DABD6			P2.13	Config 3, 4
8	DABD7			P2.14	Config 3, 4
8	XWSBD1			P3.0	Config 3, 4
8	XCLBD1			P3.1	Config 3, 4
8	XWSBD0			P3.2	Config 3, 4
8	XCLBD0			P3.3	Config 3, 4

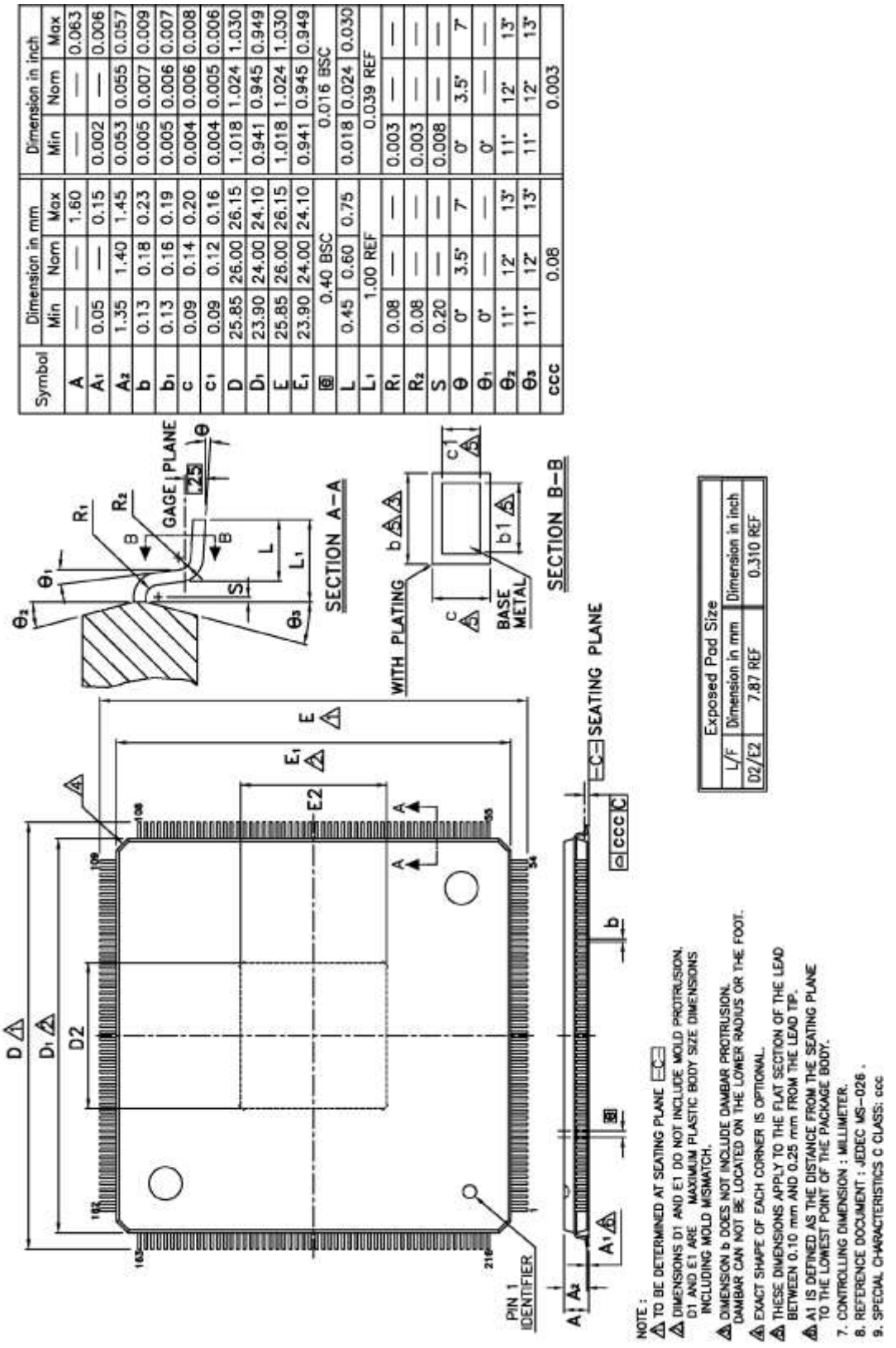
(To be continued)

(Continued)

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	USB Port 0				
17	OSC1_X1-OSC1_X2				Config 1-4
17	USBDP0-USBDM0				Config 1-4
17	USBREF0				Config 1-4
17	USBID	5	MIDI_OUT2	P8,15	Config 1-4
	USB Port 1				
18	USBDP1-USBDM1				Config 1-4
18	USBREF1				Config 1-4
	Pure GPIOs				
	P3.7			P3.7	Config 2
	P4.8-P4.15			P4.8-P4.15	Config 4
	P5.7			P5.7	Config 3, 4
	P5.8			P5.8	Config 3, 4
	P5.9			P5.9	Config 3, 4
	P5.10			P5.10	Config 3, 4
	P5.11			P5.11	Config 3, 4
	P6.5			P6.5	Config 3, 4
	P6.6			P6.6	Config 3, 4

5. Mechanical dimensions

216-pin LQFP Package



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc		0.08			0.003	

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D2/E2	7.87 REF	0.310 REF

NOTE :
1. TO BE DETERMINED AT SEATING PLANE -C-
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 .
9. SPECIAL CHARACTERISTICS C CLASS: ccc

dream	ZI 21140 Semur-en-Auxois FRANCE	**TITLE** **216LD E-PAD LQFP (24x24x1.4mm)** **Package Outline -CU L/F** - L/F Material: C7025 1/2H - Foot Print: 2 mm	**Package designation** EL216-24x24-01	**REV.** **B**

6. Marking

LQFP216

7. Electrical Characteristics

7.1. Absolute Maximum Ratings(*)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on 5 volt tolerant pin (5VT):	-	-0.3	-	5.5	V
Voltage on pin supplied by VM (MEM):	-	-0.3	-	VM+0.3	V
Voltage on standard pin supplied by VD33:	-	-0.3	-	VD33+0.3	V
Supply voltage	VD12	-0.3	-	1.32	V
	VC12	-0.3	-	1.32	V
	VD33	-0.3	-	3.63	V
	VM	-0.3	-	3.63	V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core supply voltage	VD12	1.1	1.2	1.3	V
PLL and DLL supply voltage	VC12	1.1	1.2	1.3	V
Periphery supply voltage	VD33	3	3.3	3.6	V
ADC supply voltage	VA33	3	3.3	3.6	V
Memory pads Supply voltage in SSTL_2 mode	VM	2.3	2.5	2.7	V
Memory pads Supply voltage in LVTTL mode	VM	3	3.3	3.6	V
Operating ambient temperature	tA	0	-	70	°C
Pull Resistor on MC[1:0] and FS[1:0] pins	RCFG	4.7k	10k	22k	Ohm

7.2.1. Memory pads

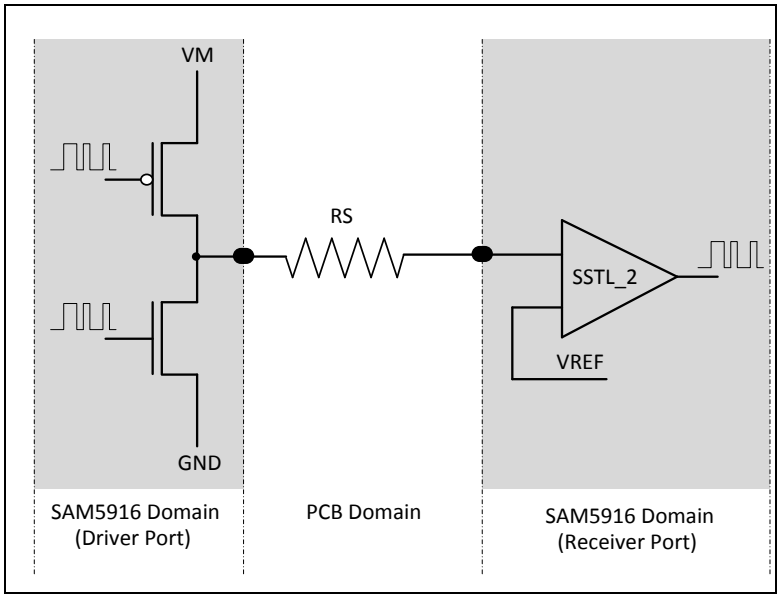
Memory pads (MEM) of SAM5916B are SSTL_2 and LVTTL compliant. This feature allows direct interfacing with DDR SDRAM and SDR SDRAM devices.

Output Drive Strength of memory pads can be selected by firmware between Low (Class1) or Medium (Class 2) or High (default).
Output Slew rate of memory pads can be selected between Fast (default) and Slow.

Note
Default setting is High drive output. However it is recommended to switch to Low drive output for all standard applications with unterminated output load.

7.2.1.1. DDR SDRAM OPERATION (SSTL_2 mode)

When using DDR SDRAM memory, it is recommended to use the following schematic for each connected memory pad.



VM = 2.5V RS= 25 Ohm VREF = 1.25V

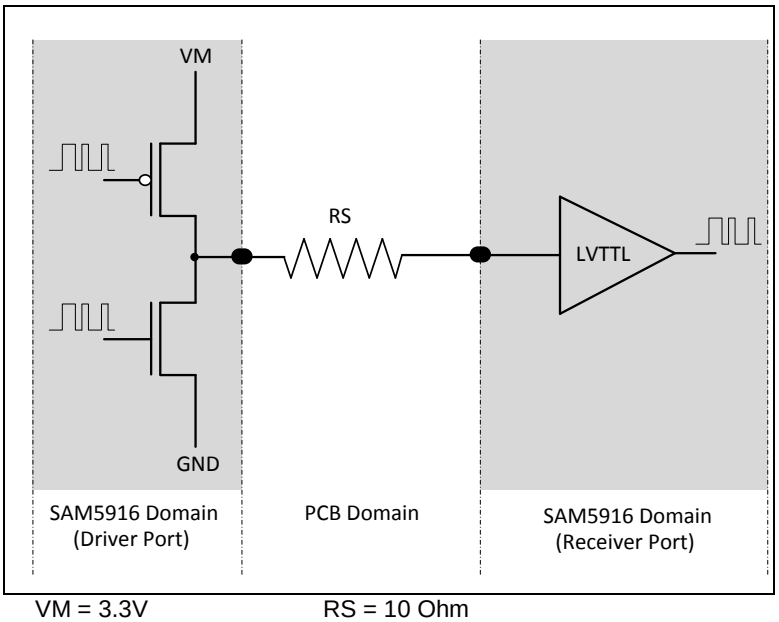
RS should be implemented in the middle of the lead-in or close to the transmitting device.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VM	2.3	2.5	2.7	V
Reference voltage	VREF	1.13	1.25	1.38	V
Serial resistor: Low drive output	RS	18	25	33	Ohm
High drive output	RS	33	47	56	Ohm

For more detail about SSTL_2, please refer to the EIA/JEDEC standard EIA/JESD8-9

7.2.1.2. SDR SDRAM, FLASH, SRAM OR GPIO OPERATION (LVTTL mode)

When using SDR SDRAM, FLASH, SRAM or GPIO signals, it is recommended to use the following schematic for each connected memory pad.



VM = 3.3V RS = 10 Ohm
VREF is not used. VREF pin can be grounded or left open.
RS should be implemented in the middle of the lead-in or close to the transmitting device.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VM	3	3.3	3.6	V
Serial resistor: High drive output	RS	8.2	10	12	Ohm

7.3. D.C. Characteristics (TA=25°C, VD12=VC12=1.2V±10%, VD33=3.3V±10%)

7.3.1. Memory pads in SSTL_2 mode (VM=2.5V±10%, VREF=1.25V±10%)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	VREF-0.31	V
High level input voltage	VIH	VREF+0.31	-	-	V
Peak-to-peak input voltage range	VIPP	0.3	-	-	V
Built-in pull-down resistor	RD	40	75	190	kOhm

7.3.2. Memory pads in LVTTL mode (VM=3.3V±10%)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage	VIH	2	-	-	V
Low level output voltage (IOL =20mA)	VOL	-	-	0.4	V
High level output voltage (IOH = 20mA)	VOH	2.4	-	-	V
Built-in pull-down resistor	RD	40	75	190	kOhm

7.3.3. Standard LVTTL pads

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage on **5VT** pins	VIH	2	-	-	V
High level input voltage on non **5VT** pins	VIH	2	-	-	V
Low level output voltage (IOL =4 ~ 12mA)	VOL	-	-	0.4	V
High level output voltage (IOH =4 ~ 12mA	VOH	2.4	-	-	V
Schmitt-trigger negative-to-threshold voltage (RST/ pin)	VTN	0.8	1.1	-	V
Schmitt-trigger positive-to-threshold voltage (RST/ pin)	VTP	-	1.6	2	V
Driving capability at VOL, VOH for **DR4** pins	IOHL	-	-	4	mA
Driving capability at VOL, VOH for **DR8** pins	IOHL	-		8	mA
Driving capability at VOL, VOH for **DR12** pins	IOHL	-		12	mA
Input leakage current	IIN	-	±1	±10	µA
Built-in pull-up / pull-down resistor	RUD	40	75	190	kOhm

7.3.4. Analog I/O pins (USBDP0, USBDM0, USBDP1, USBDM1)

Parameter	Symbol	Min	Typ	Max	Unit
High-speed differential input sensitivity VI(USBDP)-VI(USBDM)	VHSDIF	300	-	-	mV
Voltage range input of the high-speed data signaling in the common mode	VHSCM	-50	-	500	mV
High-speed idle-level output voltage (Differential)	VHSOI	-10	-	10	mV
High-speed low-level output voltage (Differential)	VHSOL	-10	-	10	mV
High-speed high-level output voltage (Differential)	VHSOH	-360	-	400	mV
Driver output impedance.	RDRV	40.5	45	49.5	Ohm

7.3.5. General Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
OUTVC12 output voltage	VD12	1.14	1.2	1.26	V
VD33 power supply current in warm power down (PLL stopped, Sys clk = 12.288MHz crystal, all P24 stopped)	ID33	-	8.9	-	mA
VD33 power supply current in reset mode (RST/=0)	ID33	-	3.6	-	mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped)	ID33		101		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 running)	ID33		250		mA
VM power supply current (crystal freq.= 12.288 MHz, VM=3.3V, SDR SDRAM)	IDM	21	-	44	mA
VM power supply current in reset mode	IDM	-	-	<1	µA
VA33 power supply current (ADC running @ 11MHz)	IA33	-	3.2	-	mA
VA33 power supply current in reset mode	IA33	-	-	<1	µA
USB Full Speed current (One USB port active)	ID33U	-	18	-	mA
USB High Speed current (One USB port active)	ID33U	-	29	-	mA
Ethernet MAC current	ID33E	-	15	-	mA

7.4. ADC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Analog bottom internal reference voltage	VRefN	-	100	150	mV
Analog top internal reference voltage	VRefP	VA33-175	VA33-125	-	mV
Resolution	RES	-	10	-	bit
Integral non-linearity error	INL	-2	±1	+2	LSB
Clock frequency	ADCCK	1	-	11	MHz
Sampling Rate	ADCSR	-	-	1	MSps

8. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by a variable multiplication factor (typ. x16) to generate the internal chip system clock ("SysClk", typ. 196.6MHz @ 12.288MHz quartz).
"spck" is the period of the internal clock. Typical value with Xtal = 12.288 MHz is spck = 5.1 ns.

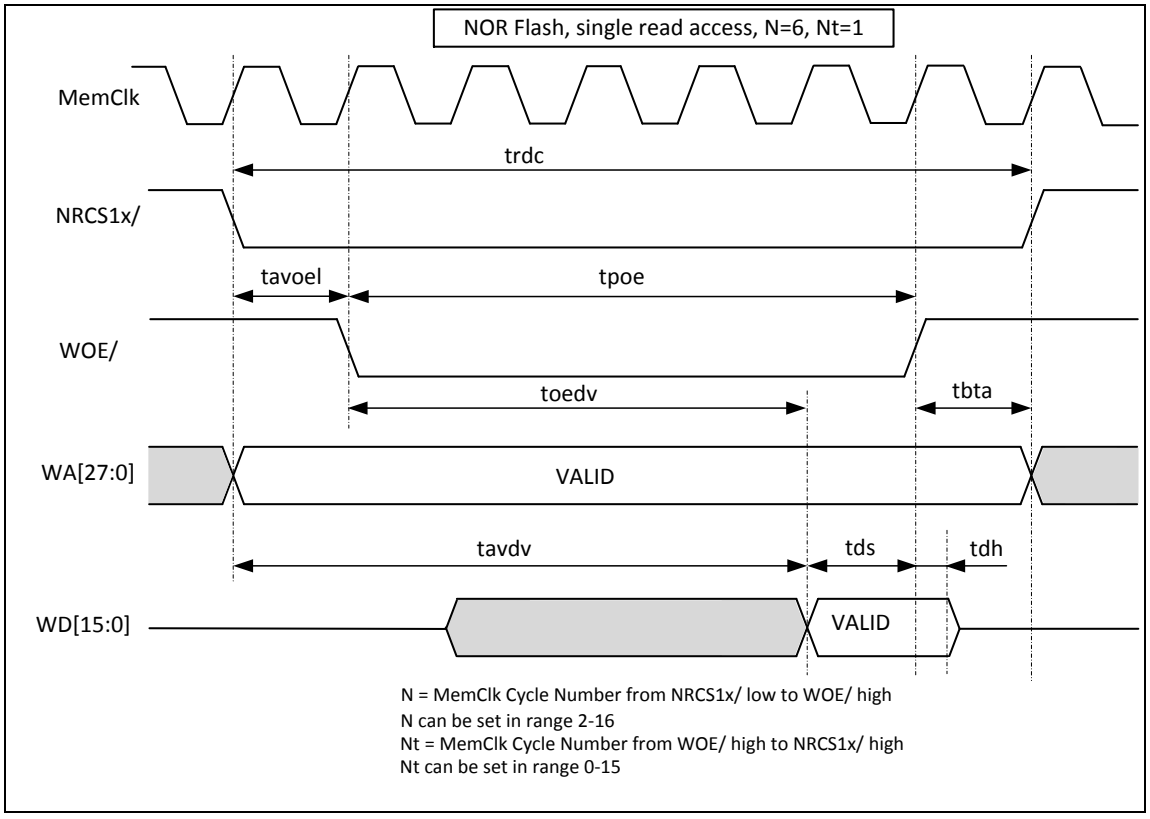
Another clock MemClk is generated from SysClk for NOR Flash, SRAM, DDR SDRAM and SDR SDRAM controllers.
mpck is the period of MemClk.
mpck = spck or spck*2. Typical values with Xtal = 12.288 MHz are mpck = 10.2 ns or 5.1 ns.

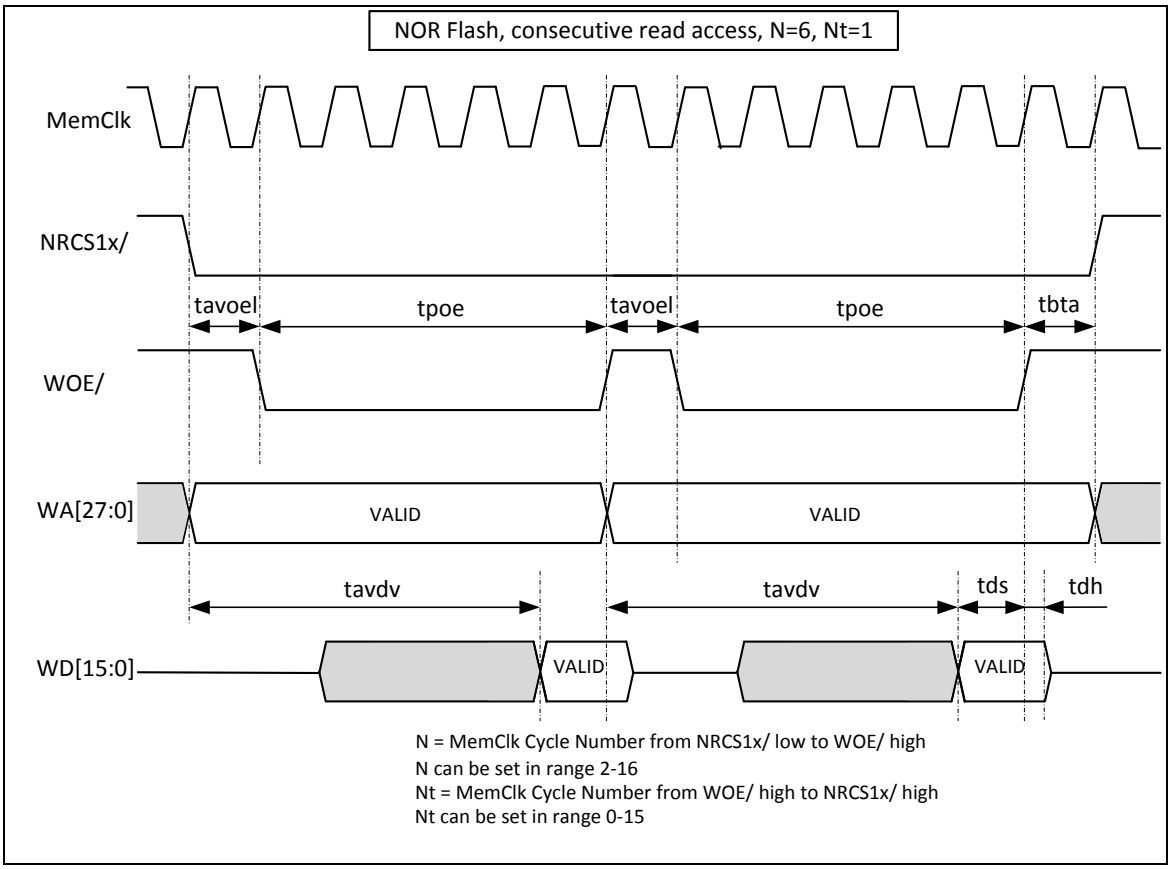
8.1. NOR Flash external memory

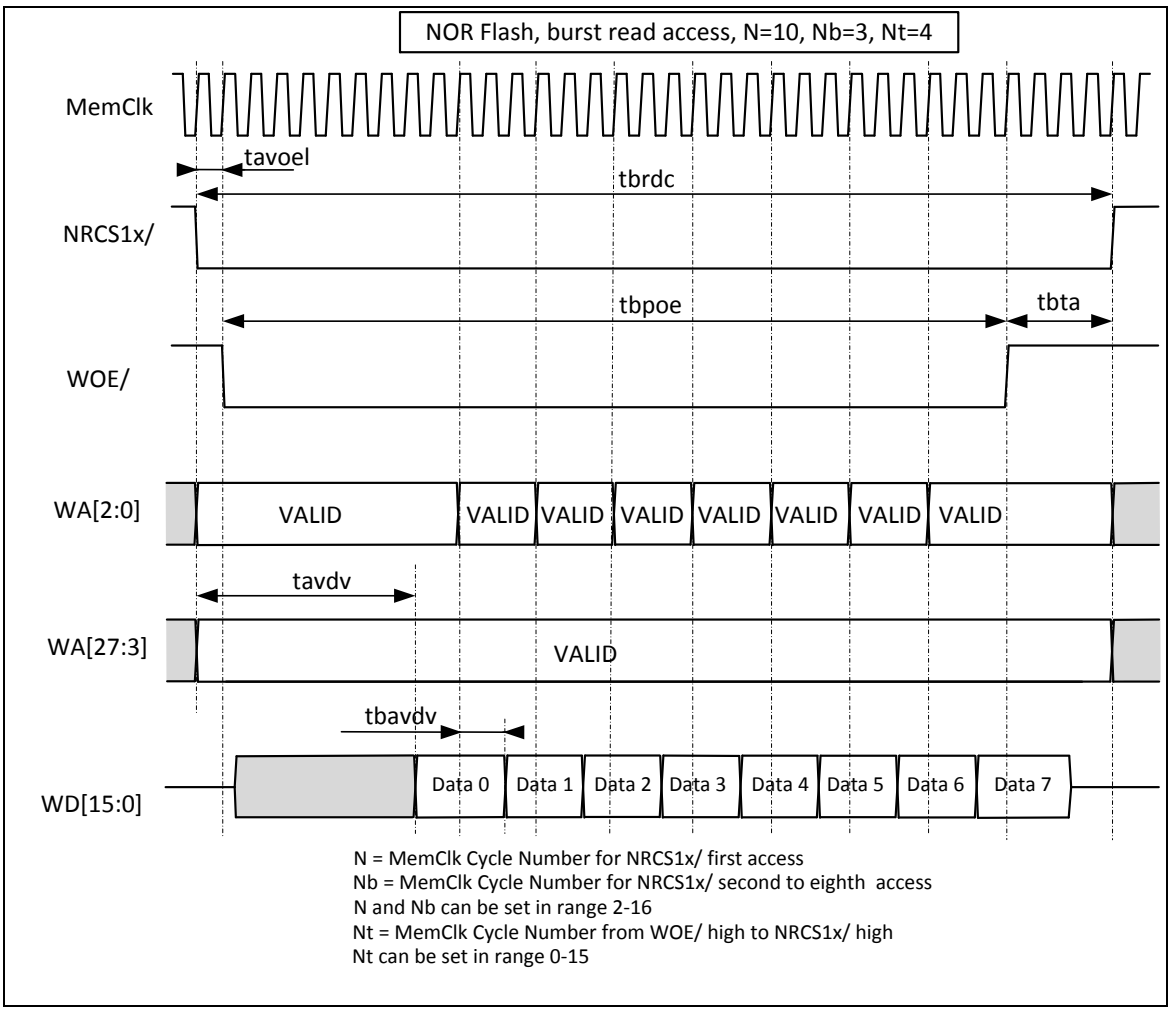
Pins used:
WA27-WA0: Address out
WD15-WD0: Data bi-directional
NRCS10/, NRCS11/, NRCS12/, NRCS13/: chip select
WOE/: Output enable
WWE/: Write enable

NRCS13/ and WA27 shared the same pin and are mutually exclusive:
- When using address bits WA26-WA0, the maximum addressing range is four pages (NRCS10/, NRCS11/, NRCS12/, NRCS13/) of 128MWords (total = 1 GByte).
- When using all address bits WA27-WA0, the maximum addressing range is three pages (NRCS10/, NRCS11/, NRCS12/) of 256 MWords (total = 1,5 GByte).

8.1.1. NOR Flash READ CYCLE



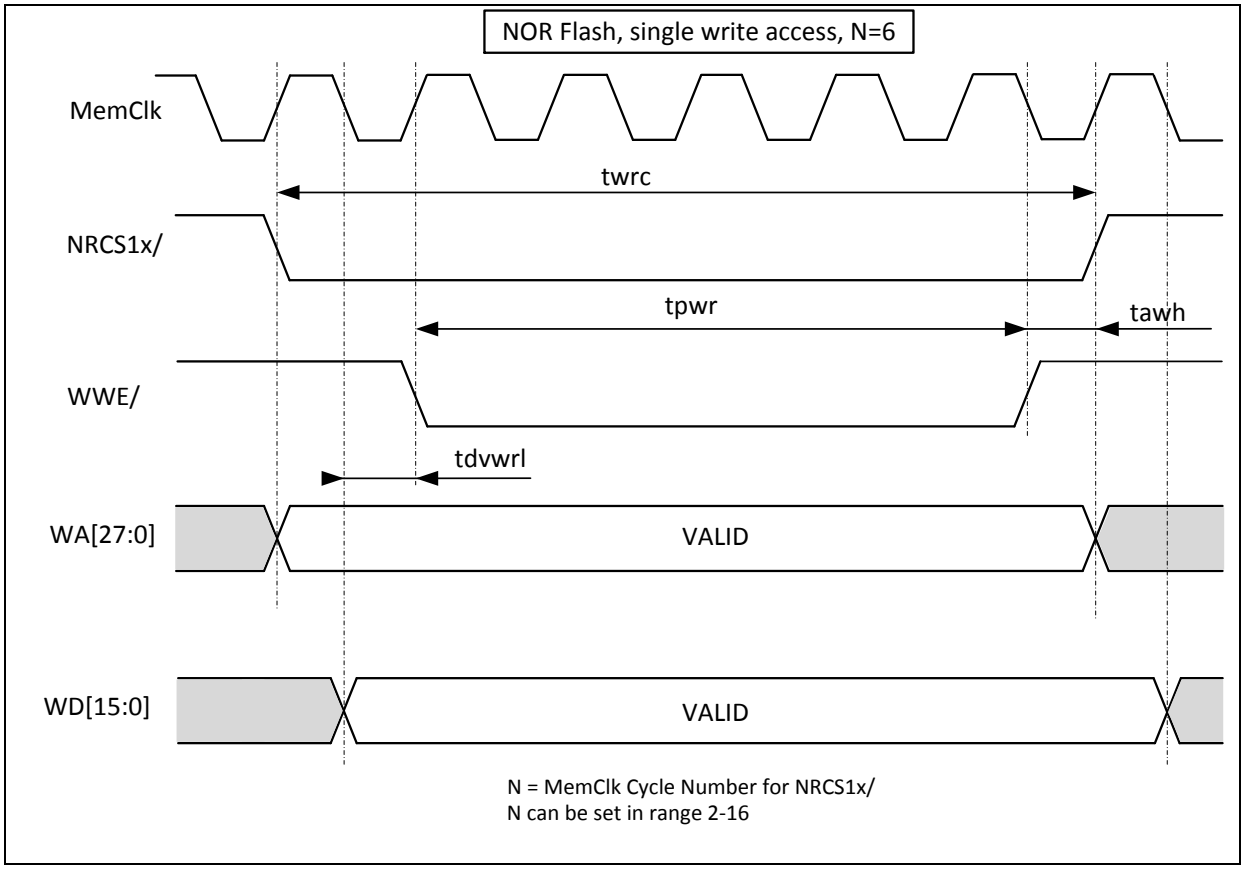


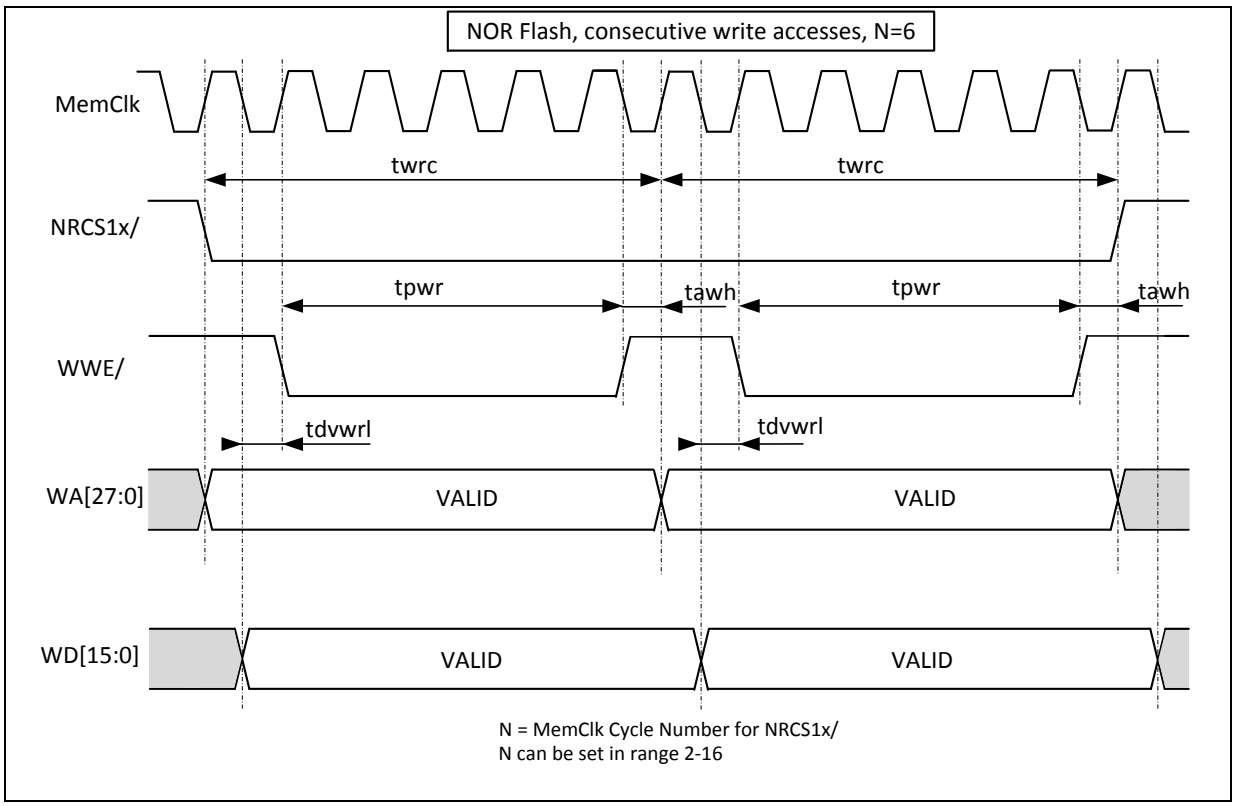


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	trdc	-	(N+Nt)*mpck	-	ns
Read cycle time in burst mode	tbdrc	-	(N+7*Nb+Nt)*mpck	-	ns
Output enable pulse width	tpoe	(N-1)*mpck - 2.5	(N-1)*mpck	-	ns
Output enable pulse width in burst mode	tbpoe	(N-1+7*Nb)*mpck-2.5	(N-1+7*Nb)*mpck	-	ns
Chip select/address valid to data valid	tavdv	0	-	N*mpck-8.5	ns
Chip select/address valid to data valid in burst mode, access 2 to 8	tbavdv	0	-	Nb*mpck-8.5	ns
Output enable valid to data valid	toedv	0	-	(N-1)*mpck-8.5	ns
Data setup	tds	6	-	-	ns
Data hold	tdh	0	-	-	ns
Bus turnaround delay	tbta	0	Nt*mpck	-	ns
Chip select/address valid to WOE/ low	tavoel	-	mpck	-	ns

Notes:
- MemClk period = mpck
- NOR Flash random access time should be lower than tavdv Max + tds Min.
- NOR Flash page access time should be lower than tbavdv Max + tds Min.

8.1.2. NOR Flash WRITE CYCLE





Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	twrc	-	N*mpck	-	ns
Write pulse width	tpwr	(N-1.5)*mpck - 2.5	(N-1.5)*mpck		ns
Data valid to MWE/ low	tdvwrl	0.5*mpck	-	-	ns
Address out hold time	tawh	0.5*mpck- 1.5	-	-	ns

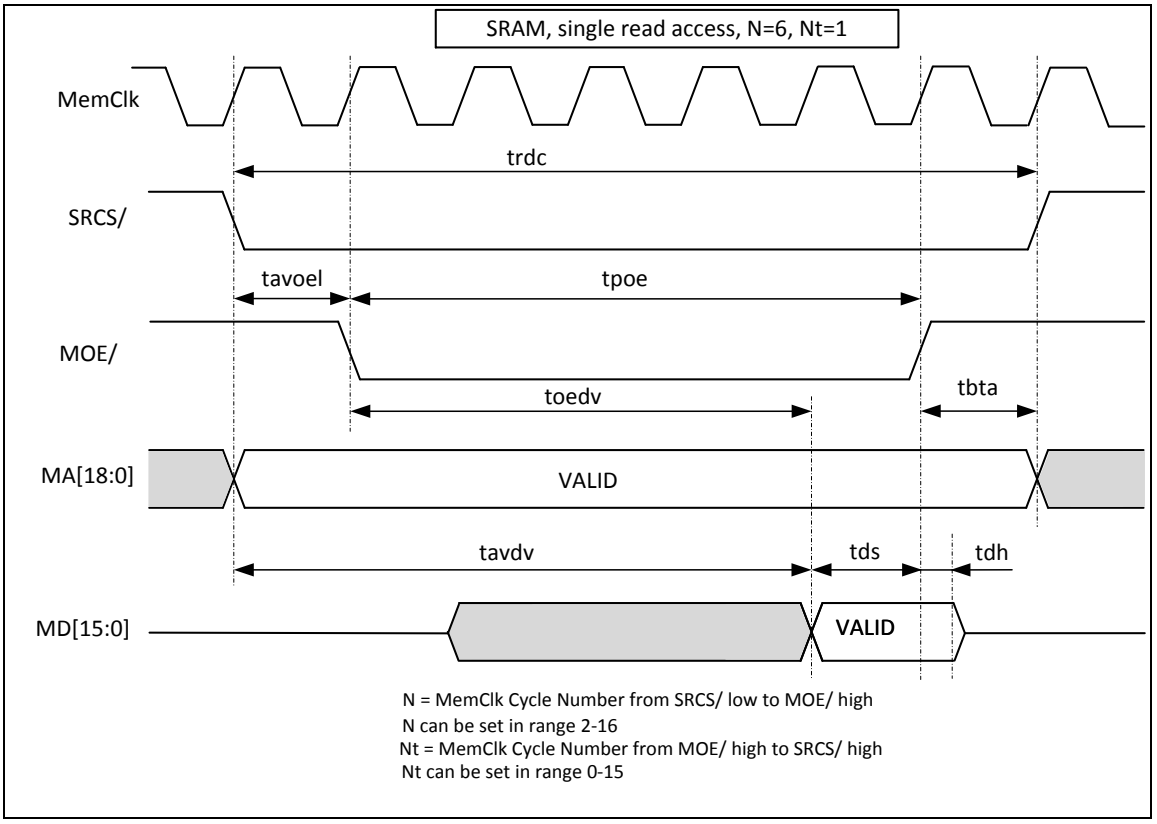
Notes:
- MemClk period = mpck

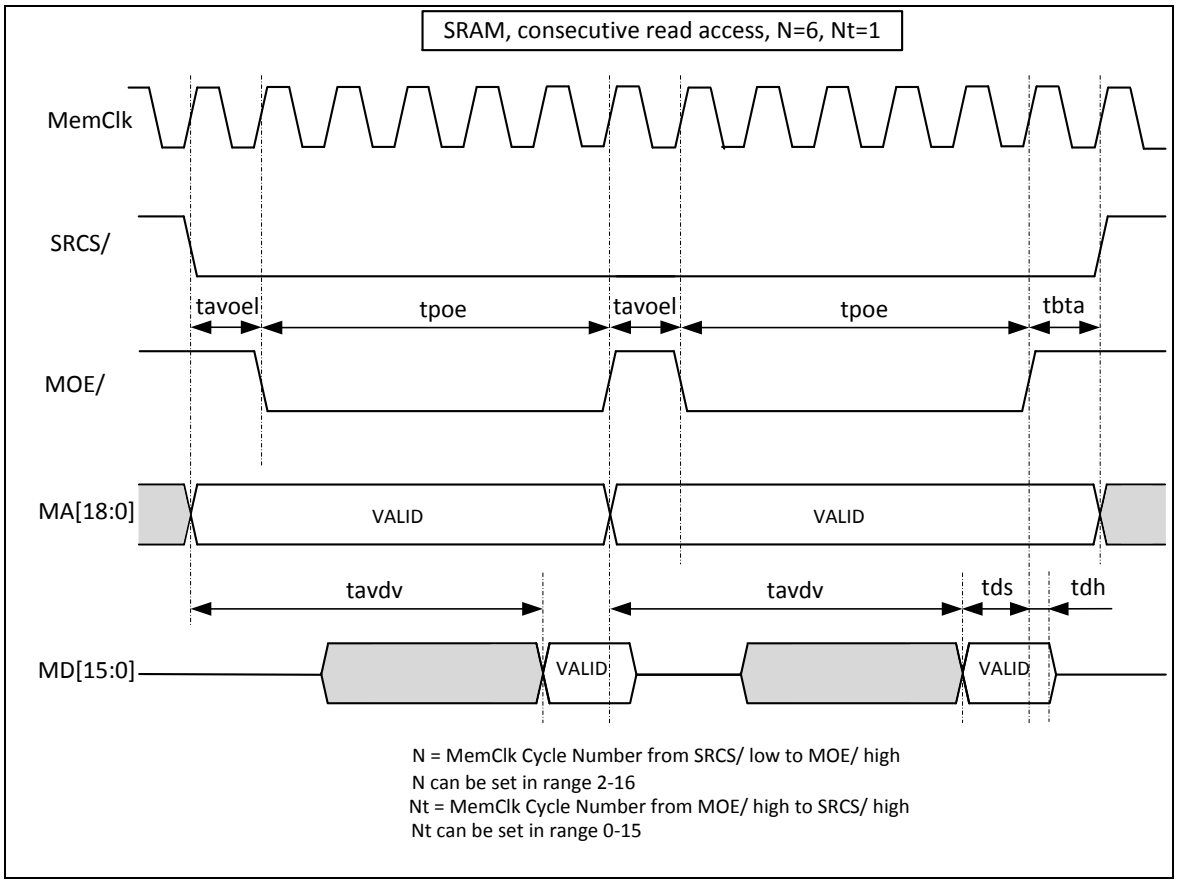
8.2. SRAM external memory

Pins used:
MA18-MA0: address out
MD15-MD0: data bi-directional
SRCS/: chip select
MOE/: output enable
MWE/: write enable

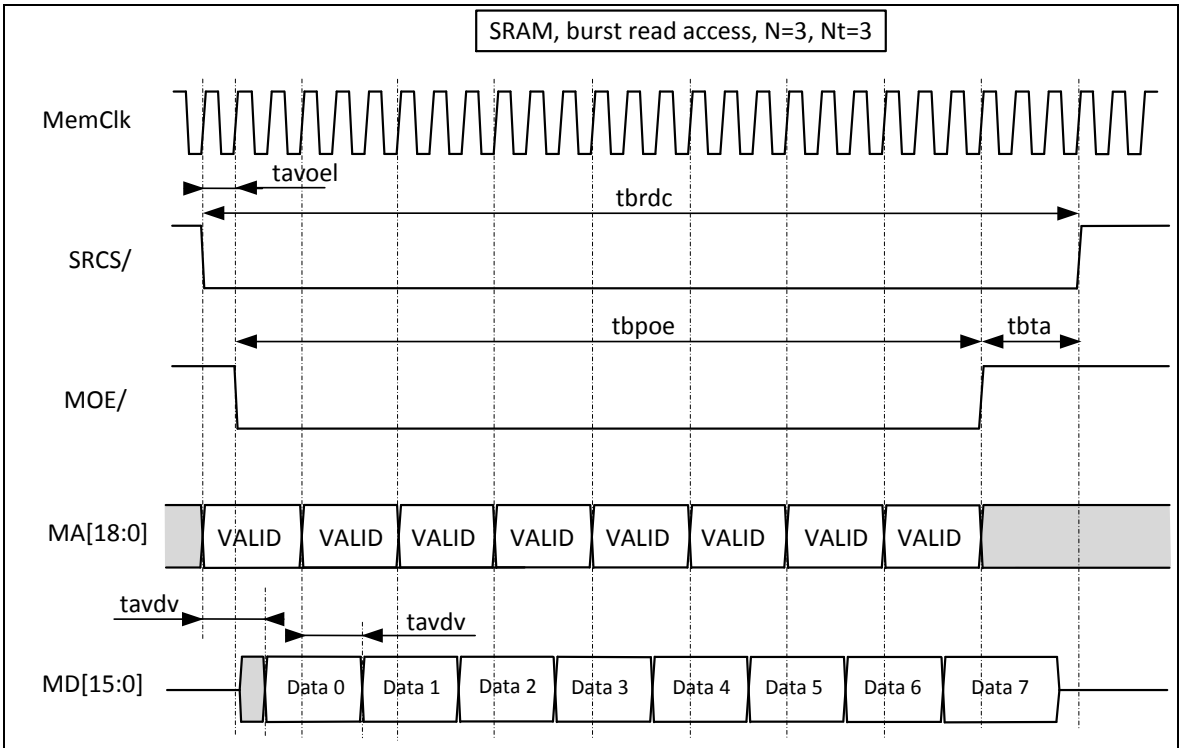
When using all address bits MA18-MA0, the maximum addressing range is 512 k x16 (8 Mbit).

8.2.1. SRAM READ CYCLE





N = MemClk Cycle Number from SRCS/ low to MOE/ high
N can be set in range 2-16
Nt = MemClk Cycle Number from MOE/ high to SRCS/ high
Nt can be set in range 0-15

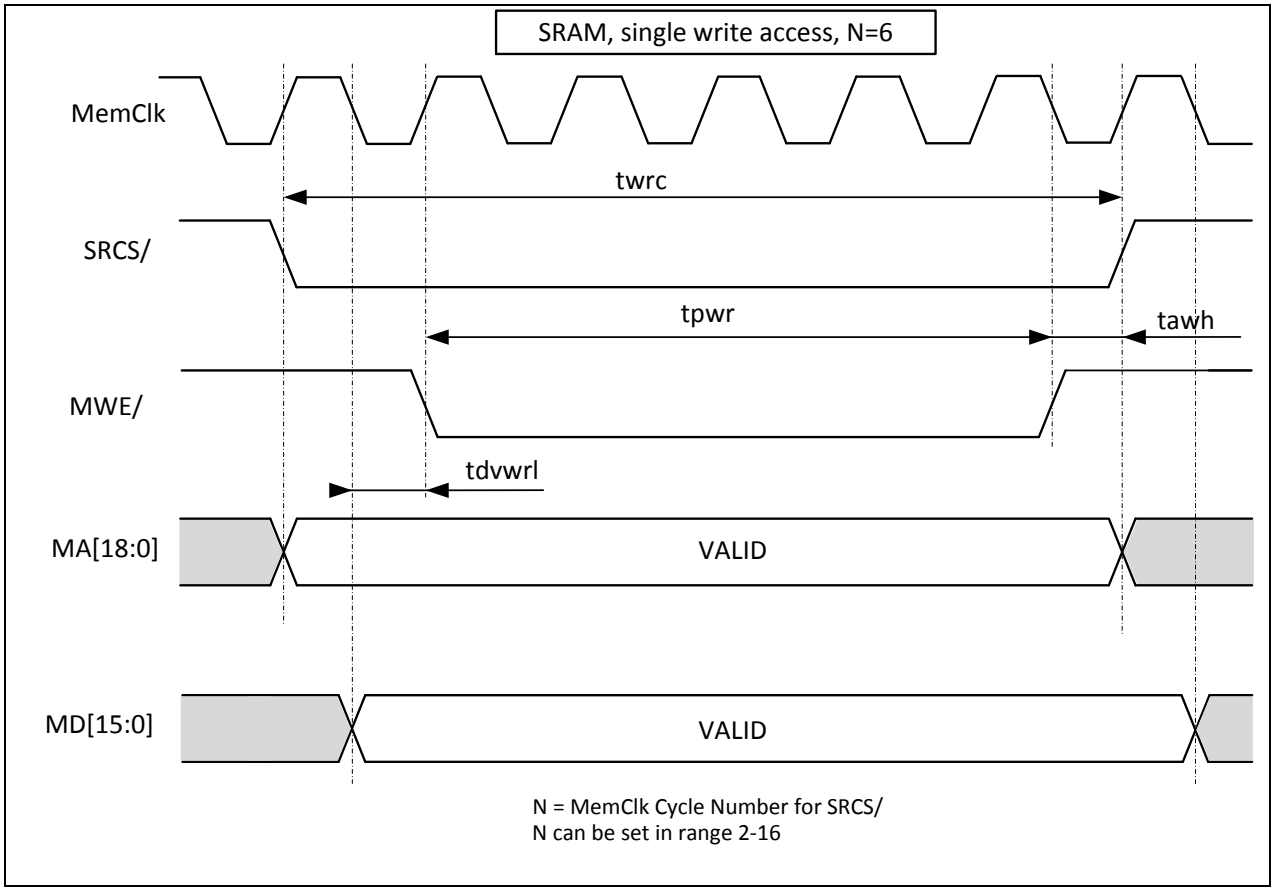


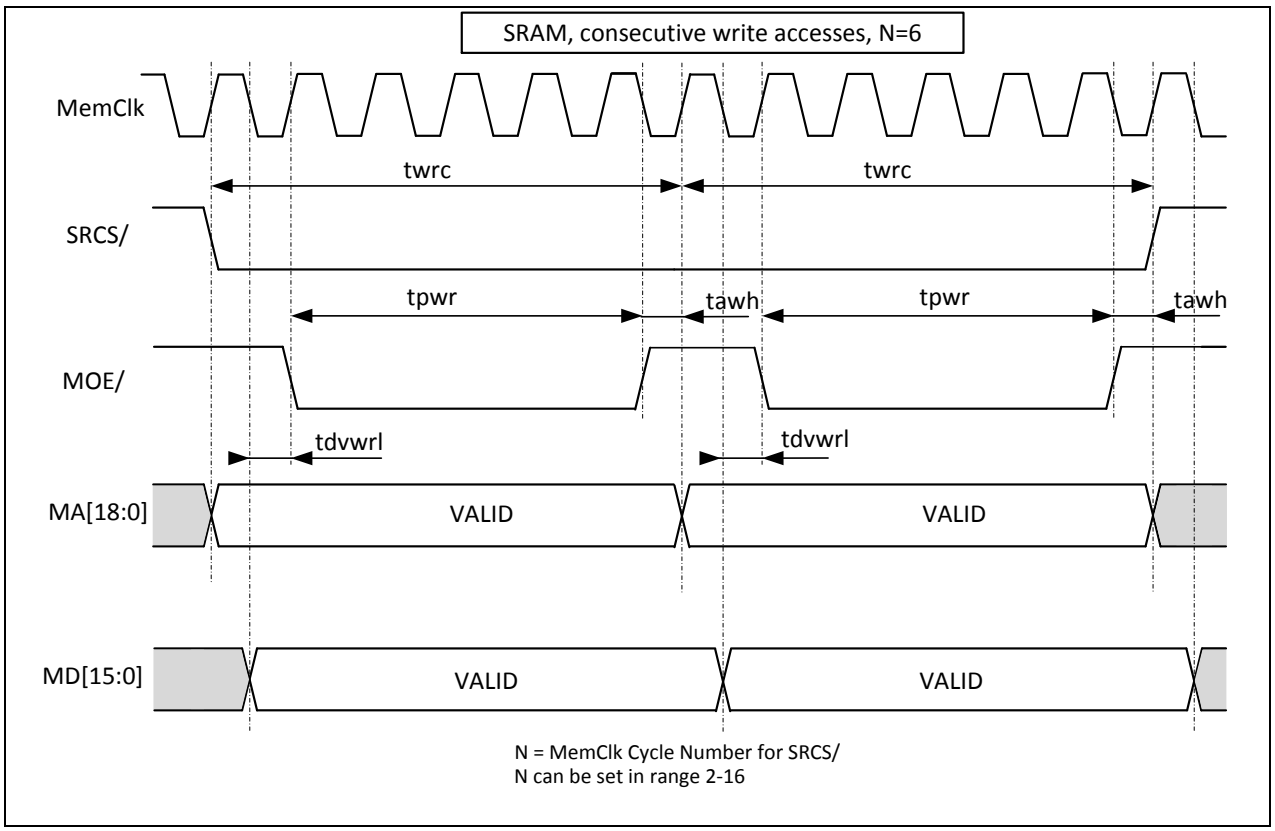
N = MemClk Cycle Number for SRCS/ first access
Nb = MemClk Cycle Number for SRCS/ second to eighth access
N and Nb can be set in range 2-16
Nt = MemClk Cycle Number from MOE/ high to SRCS/ high
Nt can be set in range 0-15

Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	trdc	-	(N+Nt)*mpck	-	ns
Read cycle time in burst mode	tbdrc	-	(N+7*Nb+Nt)*mpck	-	ns
Output enable pulse width	tpoe	(N-1)*mpck - 2.5	(N-1)*mpck	-	ns
Output enable pulse width in burst mode	tbpoe	(N-1+7*Nb)*mpck-2.5	(N-1+7*Nb)*mpck	-	ns
Chip select/address valid to data valid	tavdv	0	-	N*mpck-8.5	ns
Output enable valid to data valid	toedv	0	-	(N-1)*mpck-8.5	ns
Data setup	tds	6	-	-	ns
Data hold	tdh	0	-	-	ns
Bus turnaround delay	tbta	0	Nt*mpck	-	ns
Chip select/address valid to WOE/ low	tavoel	-	mpck	-	ns

Notes:
- MemClk period = mpck
- SRAM access time should be lower than tavdv Max + Tds Min.

8.2.2. SRAM WRITE CYCLE





Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	twrc	-	N*mpck	-	ns
Write pulse width	tpwr	(N-1.5)*mpck - 2.5	(N-1.5)*mpck		ns
Data valid to MWE/ low	tdvwrl	0.5*mpck	-	-	ns
Address out hold time	tawh	0.5*mpck- 1.5	-	-	ns

Notes:
- MemClk period = mpck

8.3. External DDR SDRAM and SDRAM memories

8.3.1. Overview

The SAM5916B supports the DDR SDRAM components compatible with JEDEC standard (JESD79F).

Following memories can be connected to the SAM5916B:

- DDR SDRAM, 16-bit wide
- SDR SDRAM, 16- bit wide

Up to four devices can be connected on chip select DRCS0/-DRCS3/.

DDR SDRAM and SDR SDRAM cannot be connected at the same time. The type of connection is SSTL_2 for DDR SDRAM. and LVTTL for SDRAM.

DDR SDRAM and SDR SDRAM use time multiplexed addressing with a ROW/COL scheme. DRA13-DRA0, DRBA1-DRBA0 are used for SDRAM addressing.

8.3.2. Address multiplexing

Number of column address bit can be set in range 8-11.
Number of row address bit can be set in range 11-14.

8.3.3. Address connection

Below is connecting table for SDR-SDRAM and DDR-SDRAM device:

SDRAM address	SAM5916B address
DA0	DRA0
DA1	DRA1
DA2	DRA2
DA3	DRA3
DA4	DRA4
DA5	DRA5
DA6	DRA6
DA7	DRA7
DA8	DRA8
DA9	DRA9
DA10	DRA10
DA11	DRA11
DA12 (if available)	DRA12
DA13 (if available)	DRA13
BA0	DRBA0
BA1	DRBA1

8.3.4. Address mapping examples

Examples below show mapping between SAM5916B SDR address pins and address bits on SAM5916B internal ASYNC bus

SDR SDRAM 16-bit wide, 64 Mbit, 12 Row addressing, 8 Column addressing

SAM5916B address pins	ASYNC bus address bits	
	Value at RAS	Value at CAS
DRA0	AAD10	AAD0
DRA1	AAD11	AAD1
DRA2	AAD12	AAD2
DRA3	AAD13	AAD5
DRA4	AAD14	AAD6
DRA5	AAD15	AAD7
DRA6	AAD16	AAD8
DRA7	AAD17	AAD9
DRA8	AAD18	Don't care
DRA9	AAD19	Don't care
DRA10	AAD20	Auto-precharge
DRA11	AAD21	Don't care
DRBA0	AAD3	AAD3
DRBA1	AAD4	AAD4

DDR SDRAM 16-bit wide, 512 Mbit, 13 Row addressing, 10 Column addressing

SAM5916B address	Value at RAS	Value at CAS
DRA0	AAD12	AAD0
DRA1	AAD13	AAD1
DRA2	AAD14	AAD2
DRA3	AAD15	AAD5
DRA4	AAD16	AAD6
DRA5	AAD17	AAD7
DRA6	AAD18	AAD8
DRA7	AAD19	AAD9
DRA8	AAD20	AAD10
DRA9	AAD21	AAD11
DRA10	AAD22	Auto-precharge
DRA11	AAD23	Don't care
DRA12	AAD24	Don't care
DRBA0	AAD3	AAD3
DRBA1	AAD4	AAD4

8.3.5. Double Data Rate SDRAM

8.3.5.1. Pinning

SAM5916B pin	DDR pin	Description
DRA[13-0]	A[13-0]	Address
DRBA1, DRBA0	BA1, BA0	Bank address
DRDQ[15-0]	DQ[15-0]	Data
DRDS1	UDQS	Data strobe (DRDQ15..DRDQ8)
DRDS0	LDQS	Data strobe (DRDQ7..DRDQ0)
DRDM1	UDQM	Data mask (DRDQ15..DRDQ8)
DRDM0	LDQM	Data mask (DRDQ7..DRDQ0)
DRCK, DRCK/	CK, CK/	Differential clock
DRCKE	CKE	Clock enable
DRCS[3-0]	CS/	Chip select. Up to 4 devices
DRCAS/	CAS/	Command
DRRAS/	RAS/	
DRWE/	WE/	
VREF	VREF	SSTL_2 reference voltage. Must be connected to 1.25 V.

8.3.5.2. Timing

General parameters

The DDR SDRAM should be used with following parameters

Parameter		Symbol	Available setting	Recommended setting
Clock cycle time		tCK	5.1ns@196.6MHz, 10.2ns@98.3MHz	10.2ns@98.3MHz
Mode Register	CAS Latency	CL	2 cycles, 3 cycles	2 cycles
	Burst length		8 data	8 data
	Burst type		sequential	sequential
	Operating mode		normal	normal
Extended mode register	DLL		enabled	enabled
	Output drive strength		low, medium, high	low
Read delay *(programmed in SAM5916B SDRAM controller)*		RDDEL	0 to 7	3-5

DDR Clock frequency

Frequency of DRCK and DRCK/ clocks is MemClk frequency.
MemClk frequency equal to SysClk or Sysclk/2.
Sysclk = Xtal * 16
Eg: Xtal = 12.288MHz and MemClk = SysClk/2 means DRCK freq = 98.3MHz

Configurations for clocks are documented in Programmer's Reference Guide ProgRef5000.pdf.

DDR timing at 200MHz

The timings below are compatible with DDR400 devices as specified in JEDEC specification JESD79F.pdf.

Timing	Min	Max	To check in DDR spec
DRCK period	5ns (200 MHz)		tCK(min)≤5 ns
DRCK duty cycle	45%	55%	
Control signals output setup to rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	1 ns		tIS(min)≤1 ns
Control signals output hold from rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	1 ns		tIH(min)≤1 ns
DQS output setup to DRCK edges (write) *(DQS outputs are DRDS[1:0])*	1.5 ns		tDSS(min)≤1.5 ns
DQS output hold from DRCK edges (write) *(DQS outputs are DRDS[1:0])*	1.5 ns		tDSH(min)≤1.5 ns
DQS output duty cycle (write) *(DQS outputs are DRDS[1:0])*	35%	65%	
DQ/DM output setup to DQS edges (write) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*	0.6 ns		tDS(min)≤0.6 ns
DQ/DM output hold from DQS edges (write) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*	0.6 ns		tDH(min)≤0.6 ns
DQ/DQS read skew (read) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*		0.6 ns	tDQSD(max)≤0.6ns

DDR timing at 100MHz

The timings below are compatible with DDR200 devices as specified in JEDEC specification JESD79F.pdf.

Timing	Min	Max	To check in DDR spec
DRCK period	10ns (100 MHz)		tCK(min)≤10 ns
DRCK duty cycle	47.5%	52.5%	
Control signals output setup to rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	3.5 ns		tIS(min)≤3.5 ns
Control signals output hold from rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	3.5 ns		tIH(min)≤3.5 ns
DQS output setup to DRCK edges (write) *(DQS outputs are DRDS[1:0])*	4 ns		tDSS(min)≤4 ns
DQS output hold from DRCK edges (write) *(DQS outputs are DRDS[1:0])*	4 ns		tDSH(min)≤4 ns
DQS output duty cycle (write) *(DQS outputs are DRDS[1:0])*	42.5%	57.5%	
DQ/DM output setup to DQS edges (write) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*	1.85 ns		tDS(min)≤1.85 ns
DQ/DM output hold from DQS edges (write) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*	1.85 ns		tDH(min)≤1.85 ns
DQ/DQS read skew (read) *(DQ outputs are DRDQ[15:0])* *(DM outputs are DRDM[1:0])*		0.8 ns	tDQSD(max)≤0.6ns

DDR fixed timing

The timings below are compatible with DDR400 devices as specified in JEDEC specification JESD79F.pdf.

Timing	Min	Max	To check in DDR spec
Active bank A to Active bank B	4 clock cycles		tRRD(min)≤4 x tCK
Mode Register Set command cycle time	2 clock cycles		tMRD(min) ≤2 x tCK
Precharge command period during initialization	4 clock cycles		tRP(min) ≤4 x tCK
Auto-Refresh command period during initialization	24 clock cycles		tMRD(min) ≤24 x tCK

There is no hard constraint on tRFC and tREFI (outside initialization - see table above). The values specified by the component can be programmed in the controller.
There is no hard constraint on tWTR. The value specified by the component must be used to compute the parameter tWTR to be programmed in the controller.
There is no hard constraint on tRC, tRAS, tRCD, tWR and tRP (outside initialization - see table above). The values specified by the component must be used to compute the parameters tRBK, tWK and tRCD to be programmed in the controller.

8.3.6. Single Data Rate SDRAM

8.3.6.1. Pinning

SAM5916B pin	SDR pin	Description
DRA[13-0]	A[13-0]	Address
DRBA1, DRBA0	BA1, BA0	Bank address
DRDQ[15-0]	DQ[15-0]	Data
DRDS[1-0]	-	Not used. Must be left unconnected
DRDM1	DQMH	Data mask (DRDQ15..DRDQ8)
DRDM0	DQML	Data mask (DRDQ7..DRDQ0)
DRCK	CK	Differential clock
DRCK/	-	Not used. Must be left unconnected
DRCKE	CKE	Clock enable
DRCS[3-0]	CS/	Chip select. Up to 4 devices
DRCAS/	CAS/	Command
DRRAS/	RAS/	
DRWE/	WE/	
VREF	-	Not used. Must be grounded or left unconnected

8.3.6.2. Timing

General parameters

The SDR SDRAM is used with following parameters

Parameter		Symbol	Available setting	Recommended setting
Clock cycle time		tCK	5.1ns@196.6MHz, 10.2ns@98.3MHz	10.2ns@98.3MHz
Mode Register	CAS Latency	CL	2 cycles	2 cycles
	Burst length		8 data	8 data
	Burst type		sequential	sequential
	Operating mode		normal	normal
Read delay *(programmed in SAM5916B SDRAM controller)*		RDDEL	0 to 7	≥ 3

SDR timing at 100MHz

Timing	Min	Max	To check in SDR spec
DRCK period	10 ns (100 MHz)		tCK(min)≤10 ns
Control signals output setup to rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	2.5 ns		tAS(min)≤2.5 ns tCKS(min)≤2.5 ns tCMS(min)≤2.5 ns
Control signals output hold from rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	1.8 ns		tAH(min)≤2.5 ns tCKH(min)≤2.5 ns tCMH(min)≤2.5 ns
Data output setup to rising DRCK (write) *MD[15:0]* *DRDM[1:0]*	2.3 ns		tDS(min)≤2.3 ns
Data output and DQM hold from rising DRCK (write) *(Data Output signals are DRDQ[15:0])* *(DQM signals areDRDM[1:0]*	1.6 ns		tDH(min)≤1.6 ns
Data input delay from rising DRCK (read) *(Data Input signals are DRDQ[15:0])*	2 ns	6.4 ns	tAC(max)≤6.4 ns tOH(min)≥2 ns
Active bank A to Active bank B	8 clock cycles		tRRD(min)≤8 x tCK
Mode Register Set command cycle time	2 clock cycles		tMRD(min) ≤2 x tCK
Precharge command period during initialization	4 clock cycles		tRP(min) ≤4 x tCK
Auto-Refresh command period during initialization	24 clock cycles		tMRD(min) ≤24 x tCK

There is no hard constraint on tRFC and tREFI (outside initialization - see table above). The values specified by the component can be programmed in the controller.
There is no hard constraint on tRC, tRAS, tRCD, tWR and tRP (outside initialization - see table above). The values specified by the component must be used to compute the parameters tRBK, tWK and tRCD to be programmed in the controller.

8.4. NAND Flash interface

8.4.1. Overview

SAM5916B can access to NAND Flash device in two ways:
- Direct communication through the NAND Flash controller. Used by P16 for NAND bad block management
- Communication through a built-in NAND Flash sequencer that will take care of transfers from the NAND Flash device to the external RAM buffer by automatically writing in NAND Flash controller registers. Used by sample cache module to feed P24 requests.

NAND Flash controller has following features:
- Handles automatic Read/write transfer through 2x2112 byte SRAM buffer
- DMA support
- Support SLC NAND Flash technology
- Programmable timing on SysClk basis
- Programmable Flash Data width 8-bit or 16-bit
- Automatic error correction while reading or writing with 4D-Hamming (up to 9 bit errors correction)
- Support Enhanced Data Output (EDO)

Pins used:
NDIO7-0: I/O for Address, Data and Command transfer on 8-bit width.
NDIO15-8: I/O extension for Address, Data and Command transfer on 16-bit width.
NDCE0/, NDCE1/: Chip Enable
NDALE: Address Latch Enable.
NDCLE: Command Latch Enable
NDWE/: Write Enable
NDRE/: Read Enable
NDR|B/: Ready Busy status

8.4.2. NAND Flash features

The NAND flash devices that can be used with SAM5916B need to have the following features:
- SLC technology
- ONFI compliant
- Read Cache Random (00h/31h) and Read Cache End commands support (3Fh)
- 2kByte or 4kByte page size
- in case of multi-plane organization, it must support interleave (multi-plane) operations and must have the 'No block address restrictions' set inside its interleaved operation attributes
- spare area at least 64 Bytes (for hamming ECC) by 2kBytes area
- page per block: 64,128, 256 or 512
- 5 address cycles max
- 8 GByte size max
- 16-bit or 8-bit bus width

8.4.3. NAND Flash external RAM buffer

When running the NAND flash sequencer, an external RAM buffer is needed to store preloaded data. Size of this buffer depends on NAND device page size and on number of used voices.
NAND management tables (64kWord) and Sound bank parameters are also stored in this RAM.

- If NAND device page size is 2kByte
  Ext. RAM size = (Voice number x 3 x 512Word) + 64kWord + Sound Bank Parameters size

- If NAND device page size is 4kByte
  Ext. RAM size = (Voice number x 3 x 1024Word) + 64kWord + Sound Bank Parameters size

8.4.4. NAND Flash controller Timing

Timing parameters of SAM5916B NAND Flash controller are programmable. They should be set according to the parameters of the connected NAND Flash. The table below helps to make the correspondence between timing parameters used by ONFI standard and timing parameters needed by the controller. The lower case parameters refer to the controller, the upper case parameters refer to ONFI standard. This table does not take in account the propagation delays on PCB.
In the tables below, the following SAM5916B timings are used:

1. tasym: Asymmetry on SAM5916B output delays (estimation: 2 ns)
2. tprop: Propagation delay inside SAM5916B (max 8 ns)

SAM5916B timing parameter	Available settings	Description	NAND Flash ONFI timing
twp	(1 to 16)* spck	Write low pulse	max(tWP, tDS) + tasym
twh	(1 to 16)* spck	Write high pulse	max(tCLH, tCH, tALH, tDH, tWH, tWC-twp) + tasym
trp	(1 to 16)* spck	Read low pulse	max(tRP, tREA) + tassym
treh	(1 to 16)* spck	Read high pulse	max(tREH, tRC-trp) + tasym
bta	(1 to 64)* spck	Bus turnaround after read	tRHZ + tasym
twsetup	(1 to 16)* spck	Write setup	max(tCLS, tCS, tALS) - twp + tasym
trsetup	(1 to 16)* spck	Read setup	max(tCEA-tREA, tCLR) + tasym
tbusy	(1 to 32)* spck	Delay after busy high	tRR – trsetup
twhr	(1 to 16)* spck	Write hold	tWHR - trsetup + tasym
tceh	(1 to 8)* spck	NDCE/ high pulse	Not constrained
ce_intercept	Disable, Enable	NDCE/ intercept enable	Disable
ce_busy	Low, High	NDCE/ level during busy	High

8.5. Multi-Purpose Quad SPI interface

This is a master synchronous serial interface, operating in Single or Quad SPI mode 0.
Quad SPI mode is driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

Single SPI mode can be driven by the QSPI controller, but also by a Simple SPI interface through two IO registers.

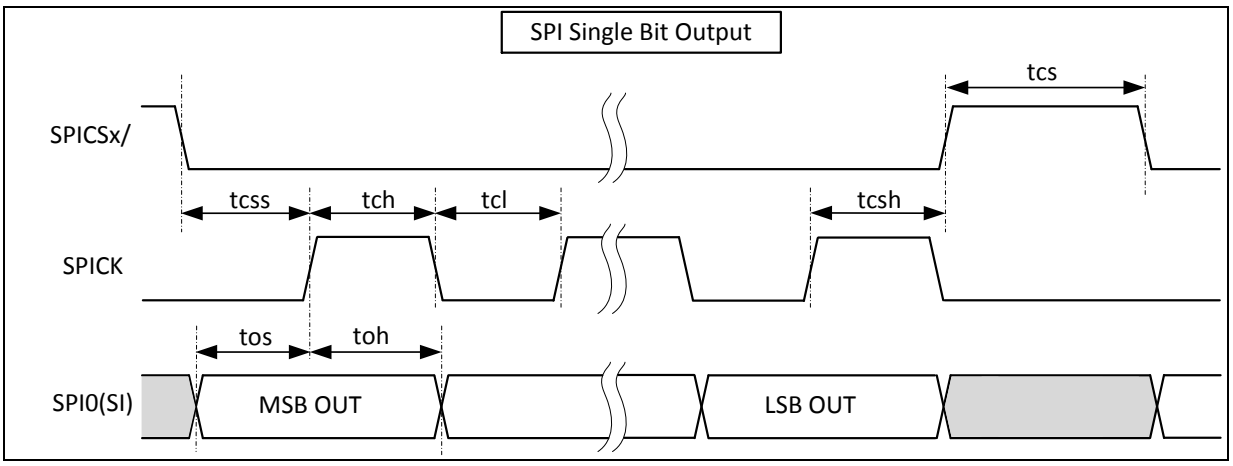
Pins used in Single SPI:

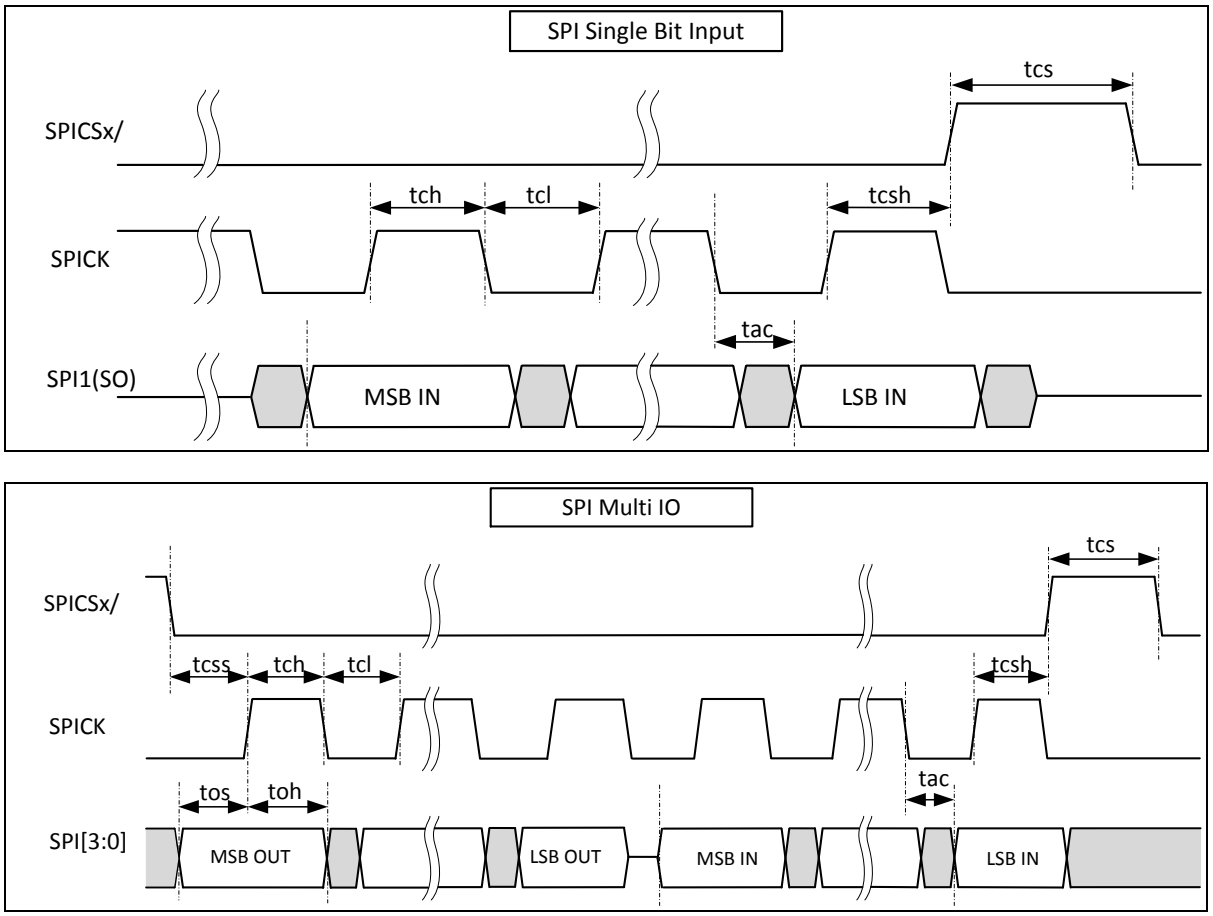
SPICK: Clock output
SPICS0/, SPICS1/, SPICS2/, SPICS3/: Chip select for up to 4 devices
SPI0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
SPI1: Serial Input to be connected to SO output of SPI peripheral (MISO

Pins used in Quad SPI:

SPICK: Clock output
SPICS0/, SPICS1/, SPICS2/, SPICS3/: Chip select for up to 4 devices
SPI0: Serial IO0 for Quad commands and data
SPI1: Serial IO1 for Quad commands and data
SPI2: Serial IO2 for Quad commands and data
SPI3: Serial IO3 for Quad commands and data

8.5.1. Timing





The QSPI controller works on SysClk (usually 196.608MHz with Xtal = 12.288MHz).
SPICK frequency is SysClk/Nq. Nq can be programmed between 2 and 4096.

Parameter	Symbol	Min	Typ	Max	Unit
SPICK Frequency	fspick	SysClk/4096	-	SysClk/2	Hz
Clock High Time (even Nq)	tch	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock High Time (odd Nq)	tch	0.5*spck*(Nq-1)-0.5		0.5*spck*(Nq-1)+0.5	ns
Clock Low Time (even Nq)	tcl	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock Low Time (odd Nq)	tcl	0.5*spck*(Nq+1)-0.5		0.5*spck*(Nq+1)+0.5	ns
CS/ High Time	tcs	spck*Nq-1.5			ns
CS/ Active Setup Time (relative to SPICK)	tcss	spck*Nq-1.5			ns
CS/ Active Hold Time (relative to SPICK)	tcsh	spck*Nq-2.5			ns
IO Out Setup Time(even Nq)	tos	0.5*spck*Nq-1.5			ns
IO Out Setup Time(odd Nq)	tos	0.5*spck*(Nq+1)-1.5			ns
IO Out Hold Time(even Nq)	toh	0.5*spck*Nq-2.5			ns
IO Out Hold Time(odd Nq)	toh	0.5*spck*(Nq-1)-2.5			ns
Access Time from falling clock edge	tac	0.5		Spck*Nq-2.5	ns

8.6. Host Parallel Interface

This interface is used to connect the SAM5916B to an external host processor for control and fast data transfer. Firmware can be downloaded at power-up through this interface.

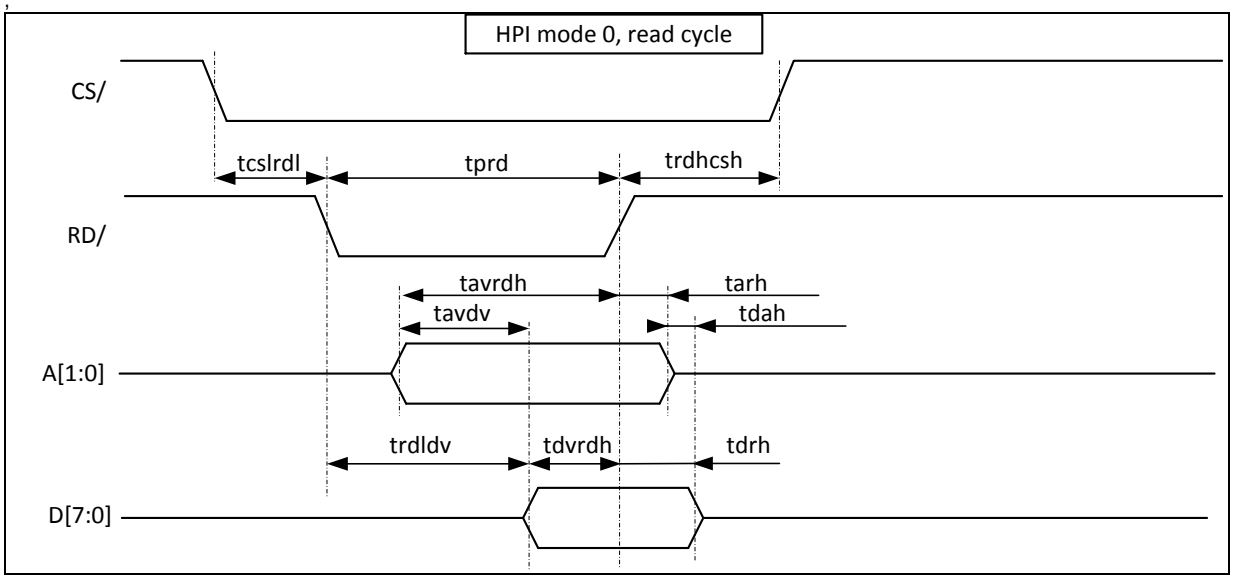
8.6.1. Host Parallel Interface (HPI) mode 0

Pins used in mode 0 (A1=0):

D7-D0: 8-bit Data I/O
CS/: Chip Select from host (input)
A1-A0: Addresses from host (input), A1=0 to select mode 0, A0 for data selection
WR/: Write from host (input)
RD/: Read from host (input)
IRQ (optional): Interrupt Request (output)

This mode is typically used to send MIDI messages or other control data from the Host CPU (master) to the SAM5916B (slave).

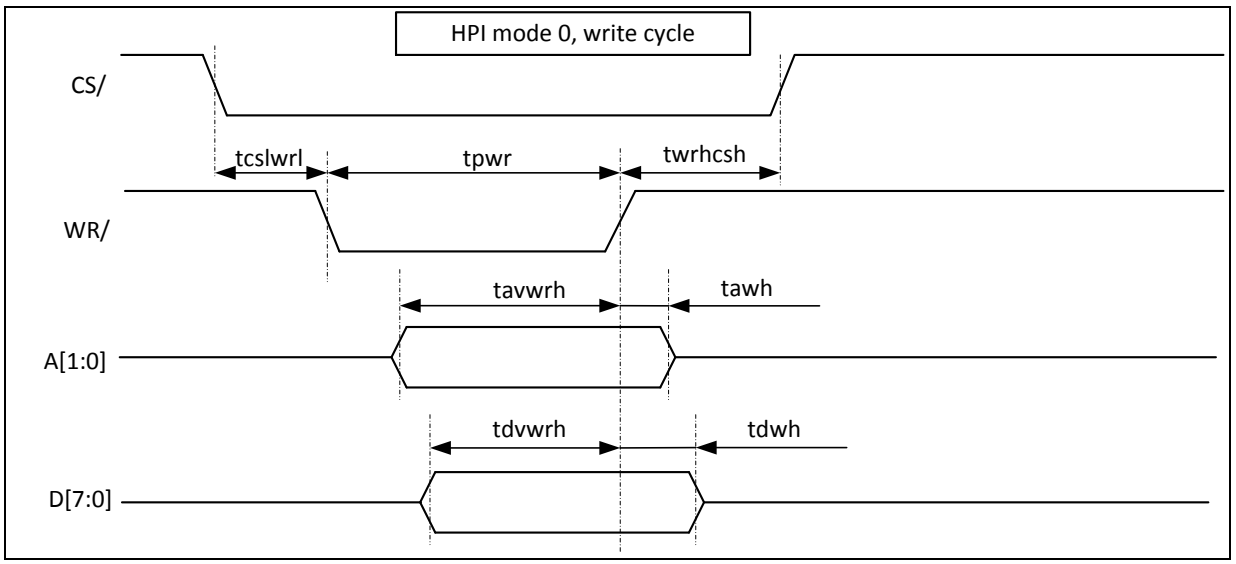
8.6.1.1. HPI mode 0, Timings



Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to RD/ low	tcslrdl	2	-	-	ns
RD/ pulse width	tprd	10	-	-	ns
RD/ high to CS/ high	trdhcsh	3	-	-	ns
Address valid to RD/ high	tavrdh	3	-	-	ns
Address valid to data valid	tavdv	-	-	10	ns
RD/ low to data valid	trdldv	-	-	10	ns
Data valid to RD/ high	tdvrdh	3	-	-	ns
Address out hold from RD/	tarh	3	-	-	ns
Data out hold from RD/	tdrh	0	-	10	ns
Data out hold from address out	tdah	0	-	10	ns

Notes:

1. tcslrdl Min and trdhcsh Min can be reduced to 0 ns if 3 ns are added to tprd Min, tarh Min, tdrh Min, tavrdh Min, tdvrdh Min



Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to WR/ low	tcslwrl	2	-	-	ns
WR/ pulse width	tpwr	5	-	-	ns
WR/ high to CS/ high	twrhcsh	3	-	-	ns
Address valid to WR/ high	tavwrh	3	-	-	ns
Data valid to WR/ high	tdvwrh	3	-	-	ns
Address out hold from WR/	tawh	3	-	-	ns
Data out hold from WR/	tdwh	3	-	-	ns

Notes:

1. tcslwrl Min and twrhcsh Min can be reduced to 0 ns if 3 ns are added to tpwr Min, tawh Min, tdwh Min, tavwrh Min, tdvwrh Min

8.6.1.2. HPI mode 0, IO Status Register

TE	RF	X	X	ID3	ID2	ID1	ID0

Status register is read when A1=0, A0=1, RD/=0, CS/=0

- TE: Transmit Empty: This bit is 1 when nothing is transmitted from SAM5916B to host. If 0, data from SAM5916B to host is pending and IRQ pin is high. Host reading the data with pin A0=0 sets TE to 1 and clear IRQ. TE bit is actually reflecting inverted value of IRQ pin (IRQ/).
- RF: Receiver Full: Host should not write any data or control to SAM5916B if this bit is 1. When 0, then SAM5916B is ready to accept data from host.
- ID[3:0]: these 4 bits are firmware dependant and may be used for defining type of data sent by SAM5916B in case of multiple flows of data.

Host read should be performed with following steps:
a) Nothing to read if IRQ pin is low. First wait for IRQ pin being high
b) Read status (A0=1) to get ID[3:0] (this step is optional if ID[3:0] bits are not used and not defined by firmware)
c) Read data (A0=0) (IRQ goes low at the end of read cycle, on rising edge of RD/ signal)
d) Wait for IRQ pin being high again…
Note: On steps a) and d), if IRQ pin is not connected and not used, host can also read status and wait for TE bit=0

Host write should be done with following steps:
a) Read status (A0=1). If bit RF=0, go to step b). If bit RF=1, read again status till bit RF going to 0.
b) Write new data (A0=0) or new control (A0=1)

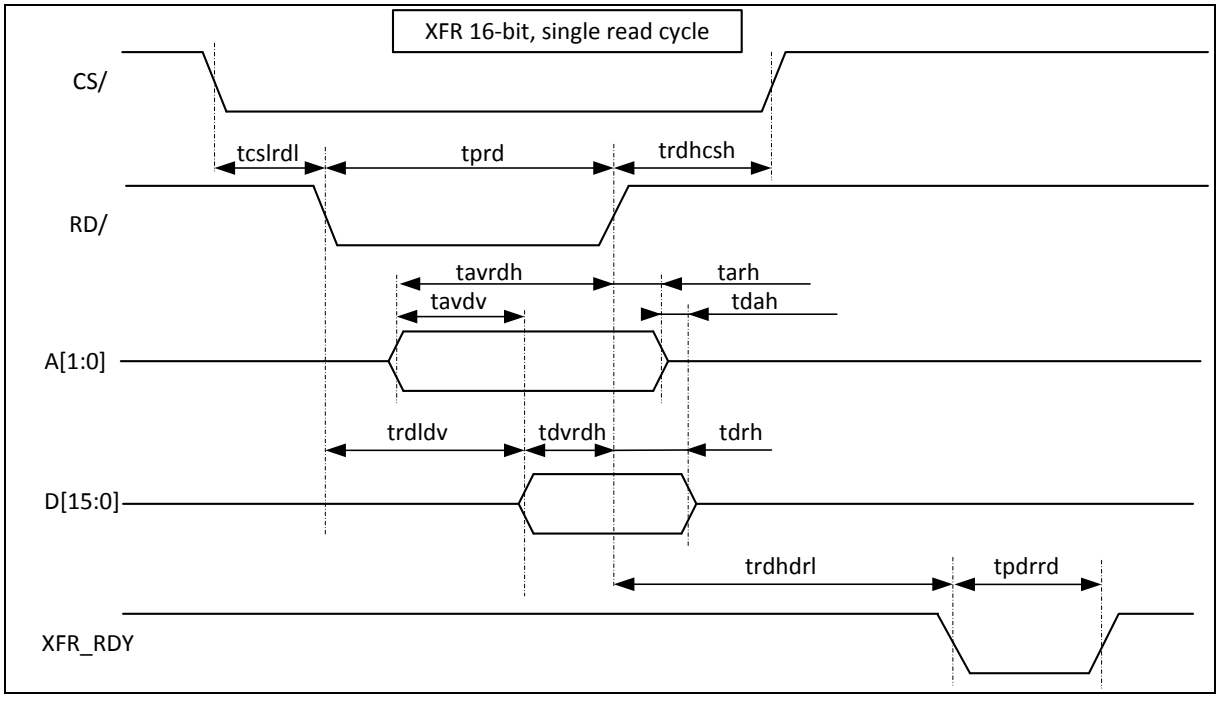
Note about step a):
There are two different cases for RF bit being 1:
- RF bit is 1 because FIFO of P16 is full. RF bit will go low again as soon as P16 is reading some bytes of the FIFO in order to have some free space again inside fifo and then is clearing bit 7 (FIFULL) of port 1 (CONTROL/STATUS). This time is firmware dependant.
- RF bit is 1 because previous host write has still not been written into the P16 FIFO. This case can happen if P16 is executing a long instruction. The writing will be indeed performed only when P16 has finished the instruction.

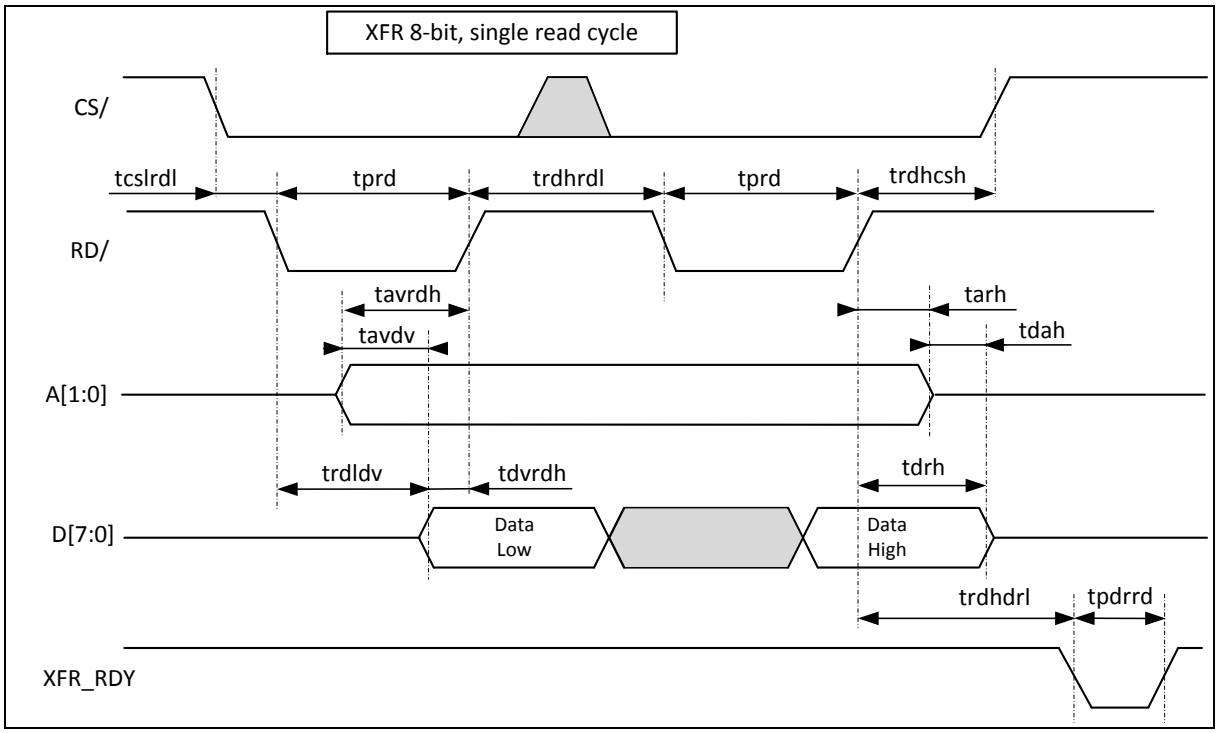
8.6.2. Host Parallel Interface mode 1 (fast data transfer)

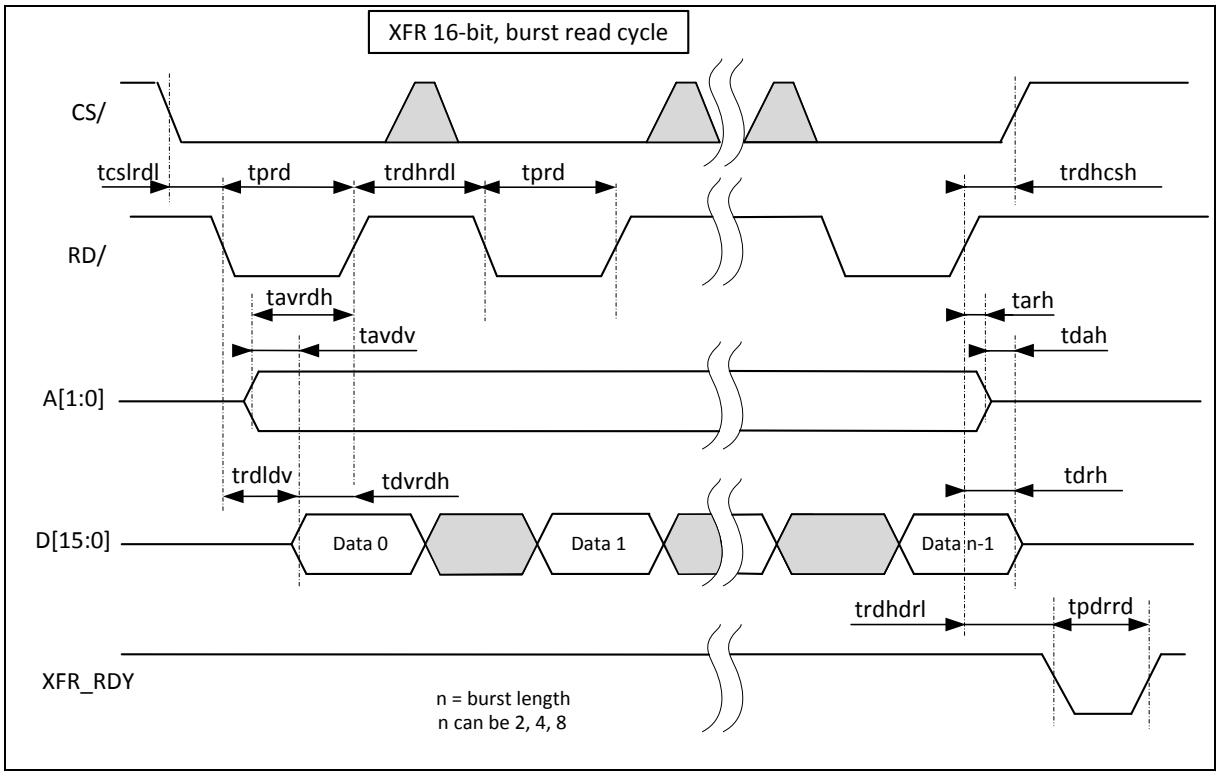
Pins used in mode 1 (A1=1):
- D7-D0 or D15-D0 (I/O)
- CS/ (input)
- A1-A0 (input): Addresses from host (input), A1=1 to select mode 1, A0 is “don’t care”.
- WR/ (input)
- RD/ (input)
- XFR_RDY (output)

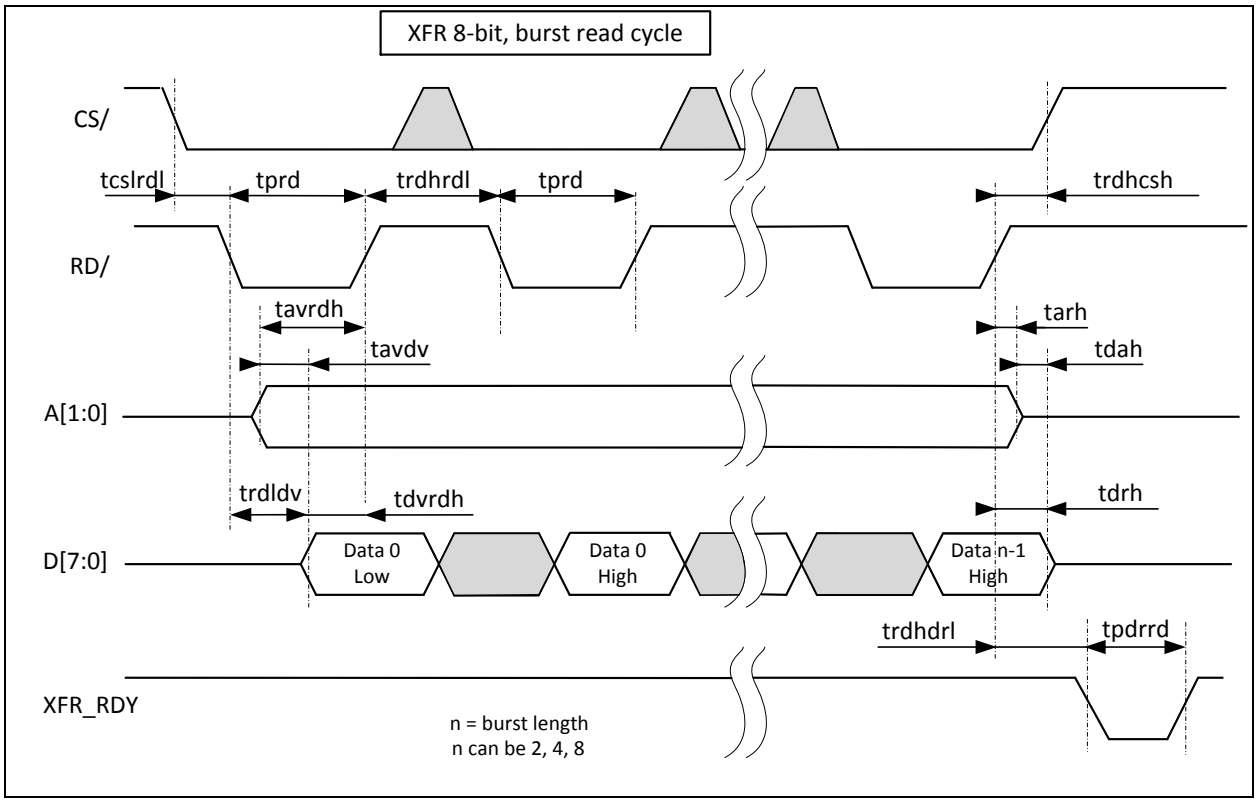
This interface is used for fast read/write transfer between host processor and SAM5916B. Typical applications are direct fast sound bank transfer from host to SDRAM and streaming audio.
However, any other devices connected to internal async bus of SAM5916B can be also accessed by host through this interface (other external memories, internal ram, router and P24 memories, etc.). Single or burst read/write modes are available. Read/write mode is selected by firmware

8.6.2.1. HPI mode 1, Read Timing







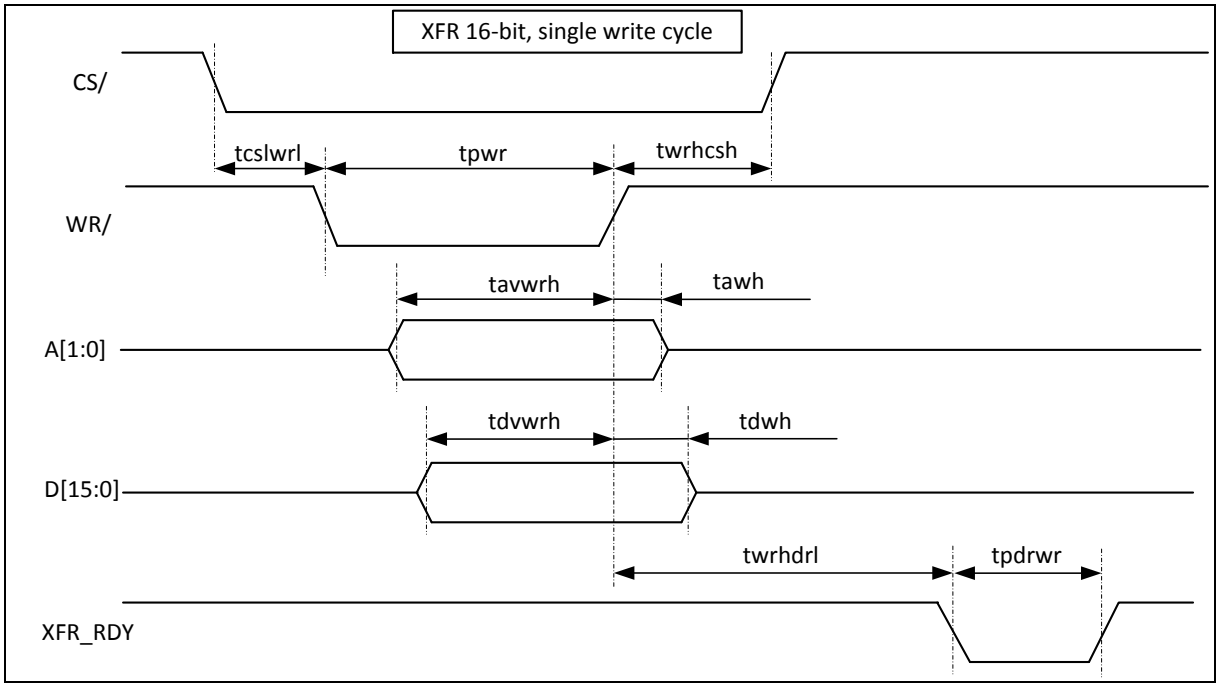


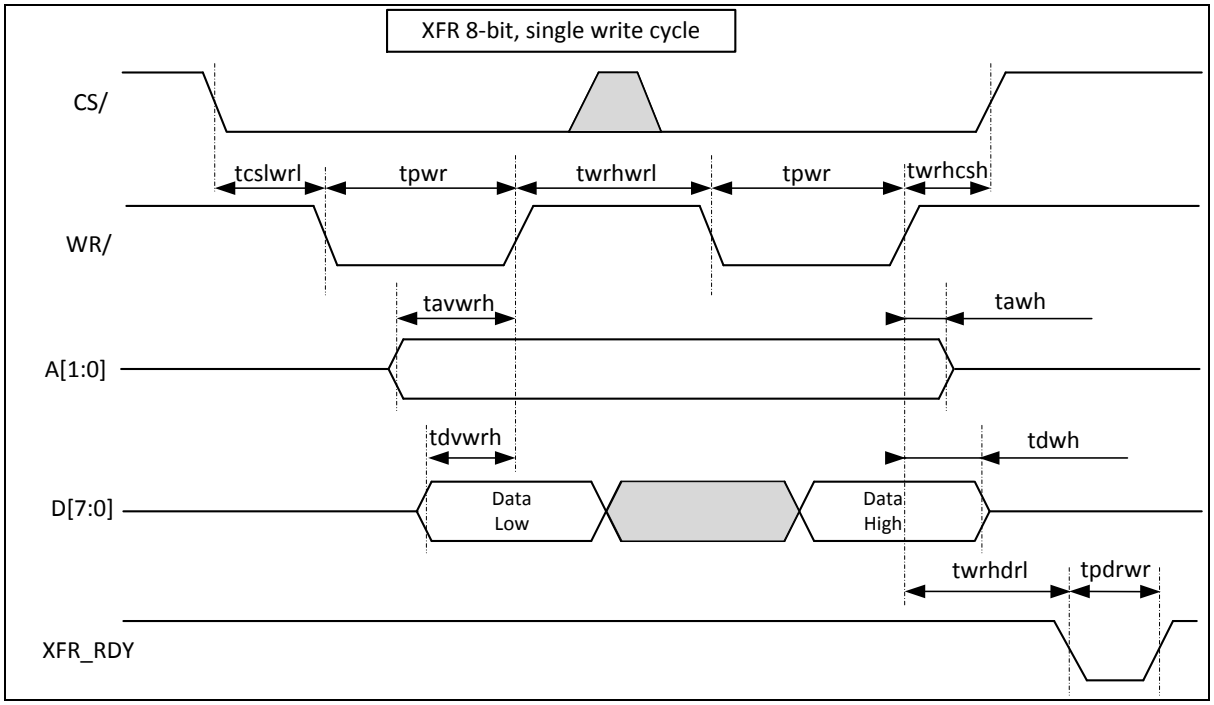
Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to RD/ low	tcslrdl	2 (see note 1)	-	-	ns
RD/ pulse width	tprd	10	-	-	ns
RD/ high to RD/ low	trdhrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	3 (see note 1)	-	-	ns
Address valid to RD/ high	tavrdh	3	-	-	ns
Address valid to data valid	tavdv	-	-	10	ns
RD/ low to data valid	trdldv	-	-	10	ns
Data valid to RD/ high	tdvrdh	3	-	-	ns
Address out hold from RD/	tarh	3	-	-	ns
Data out hold from RD/	tdrh	0	-	10	ns
Data out hold from address out	tdah	0	-	10	ns
RD/ high to XFR_RDY low	trdhdrl	-	-	10	ns
XFR_RDY pulse width in read mode	tpdrrd	15	-	-	ns

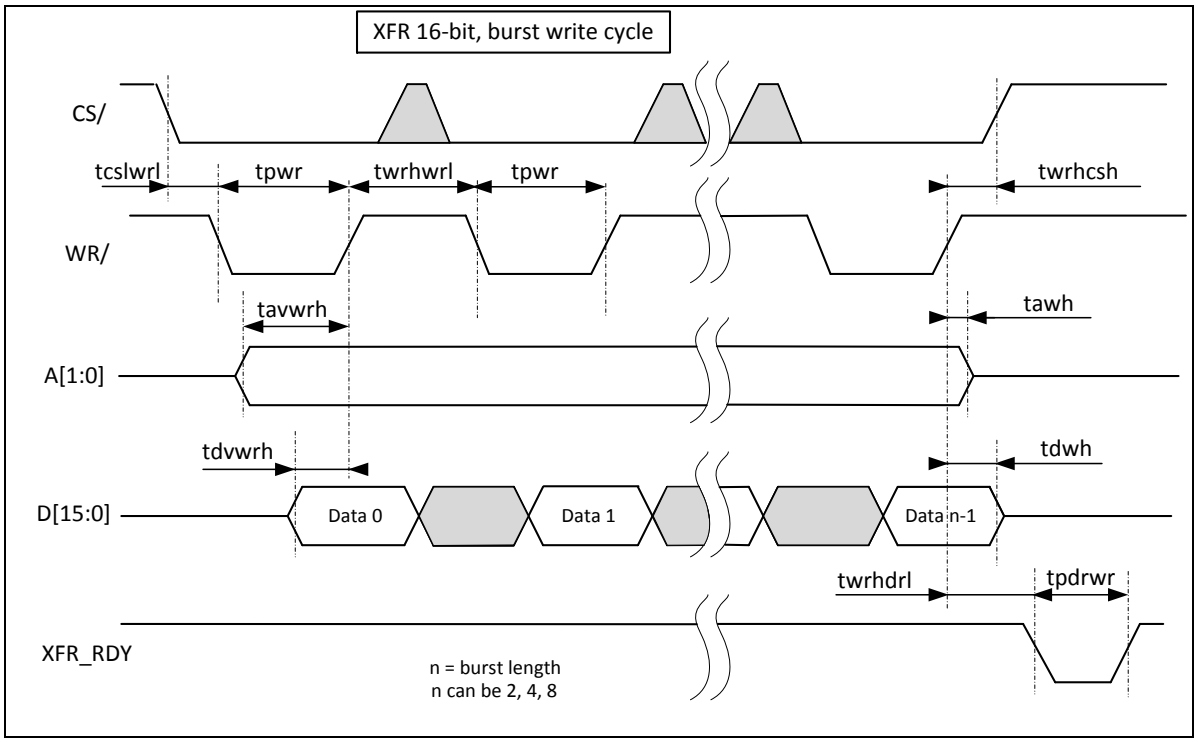
Notes:

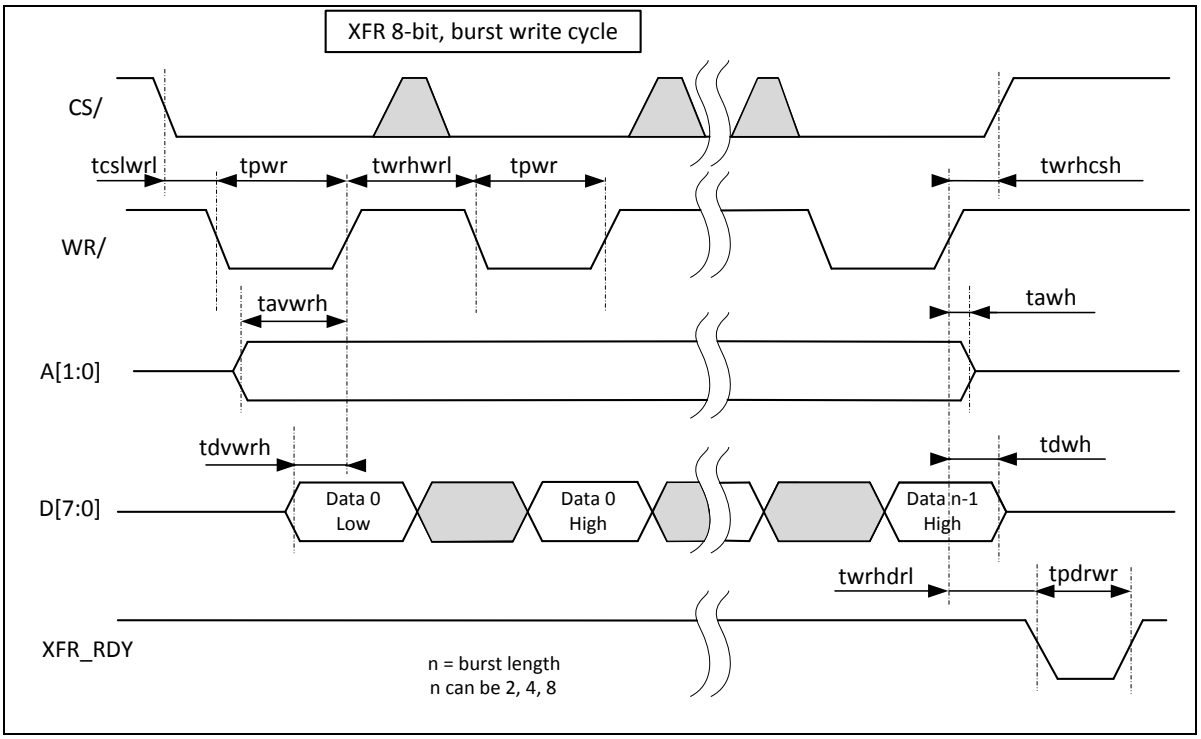
2. tcslrdl Min and trdhcsh Min can be reduced to 0 ns if 3 ns are added to tprd Min, tarh Min, tdrh Min, tavrdh Min, tdvrdh Min
3. See also §8.6.2.3 Typical timing examples

8.6.2.2. HPI mode 1, Write Timing









Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to WR/ low	tcslwrl	2 (see note 1)	-	-	ns
WR/ pulse width	tpwr	5	-	-	ns
WR/ high to WR/ low	twrhwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	3 (see note 1)	-	-	ns
Address valid to WR/ high	tavwrh	3	-	-	ns
Data valid to WR/ high	tdvwrh	3	-	-	ns
Address out hold from WR/	tawh	3	-	-	ns
Data out hold from WR/	tdwh	3	-	-	ns
WR/ high to XFR_RDY low	twrhdrl	-	-	10	ns
XFR_RDY pulse width in write mode	tpdrwr	15	-	-	ns

Notes:

2. tcslwrl Min and twrhcsh Min can be reduced to 0 ns if 3 ns are added to tpwr Min, tawh Min, tdwh Min, tavwrh Min, tdvwrh Min

8.6.2.3. Typical timing examples for sound bank loading via HPI mode 1

1) SDRAM, burst x8, 8 bit mode, no traffic (all P24 stopped)
XFR_READY low typ = 15 to 45 ns
Time for transferring 1Kx16: Write mode=25us, Read mode=32us
---> write a 256Mx16 sound bank = less than 7 seconds

2) DDR-SDRAM, burst x8, 8 bit mode, no traffic (all P24 stopped)
XFR_READY low typ = 15ns
Time for transferring 1Kx16: Write mode=25us, Read mode=32us
---> write full 256Mx16 sound bank = less than 7 seconds

3) SDRAM, burst x8, 16 bit mode, high traffic (all P24 on, 256 voice poly accessing also SDRAM simultaneously)
XFR_READY low typ = 250ns to 400ns (write mode), 150ns to 250ns (read mode)
Time for transferring 1Kx16: Write mode=47us, Read mode=37us
---> write full 256Mx16 sound bank = less than 14 seconds

8.7. Serial Slave Asynchronous Interface (UART / MIDI)

The SAM5916B can be controlled by an external host processor through this bidirectional serial interface.

Pins used:
MIDI_IN1, MIDI_OUT1: UART / MIDI port 1
MIDI_IN2, MIDI_OUT2: UART / MIDI port 2

The serial signals on MIDI_IN and MIDI_OUT pins are asynchronous signals following the UART / MIDI transmission standard:

Baud rate: programmable up to >400kb/s, typically 31.25 kb/s (MIDI) or 38.4kb/s (COM)
Format: start bit (0), 8 data bits, stop bit (1)

8.8. Serial Slave Synchronous Interface

The SAM5916B can be controlled by an external host processor through this unidirectional serial interface.

Pins used:
SSCLK, SSYNC, SSDIN (input)
SSINT/ (output)

Data is shifted MSB first. SAM5916B samples an incoming SSDIN bit on the rising edge of SSCLK, therefore the host should change SSDIN on the negative SCLK edge.

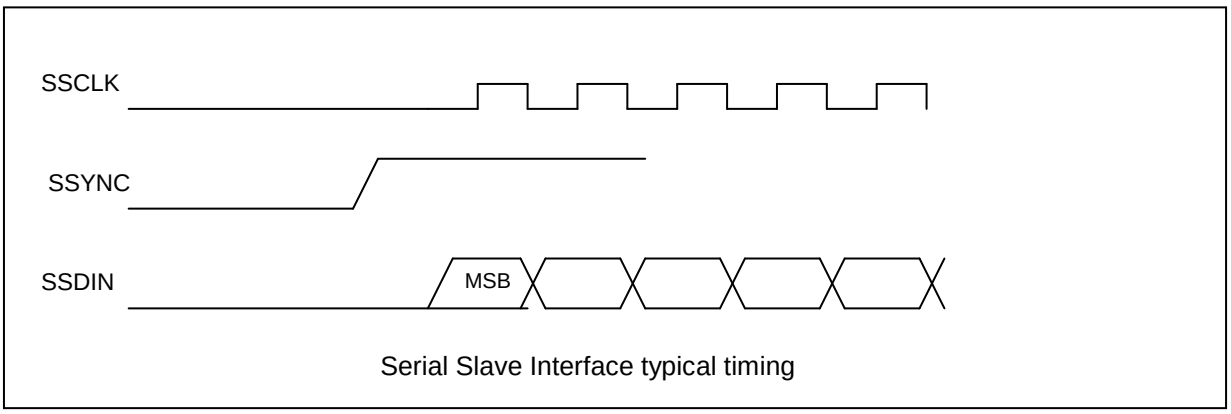
SSYNC allows initial synchronization. The rising edge of SSYNC, which should occur with SSCLK low, indicates that SSDIN will hold MSB data on the next rising SSCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependent. Minimum size is 128 bytes. Host should stop sending data as soon as SSINT/ goes high.

When the FIFO count is below 64, the SSINT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SSCLK frequency is fsck/4 (fsck being the system clock frequency. fsck =1/spck).
The minimum time between two bytes is 256 spck.

The contents of the SSDIN data are defined by the firmware.



Serial Slave Interface typical timing

8.9. I²S Digital audio

Pins used:
CLBD, WSBD (outputs): Audio clocks
DABD7-0: Digital audio outputs (8 * 2 channels)
DAAD7-0: Digital audio inputs(8 * 2 channels)

And optionally
XCLBD0-XWSBD0, XCLBD0-XWSBD0 (inputs): 2 pairs of external clocks for slave mode on DAAD7-0 inputs.

The SAM5916B allows for 16 digital audio output channels and 16 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD7-0 inputs can be individually synchronized with incoming XCLBD and XWSBD signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S or MSB left standard, with up to 24 bits per sample

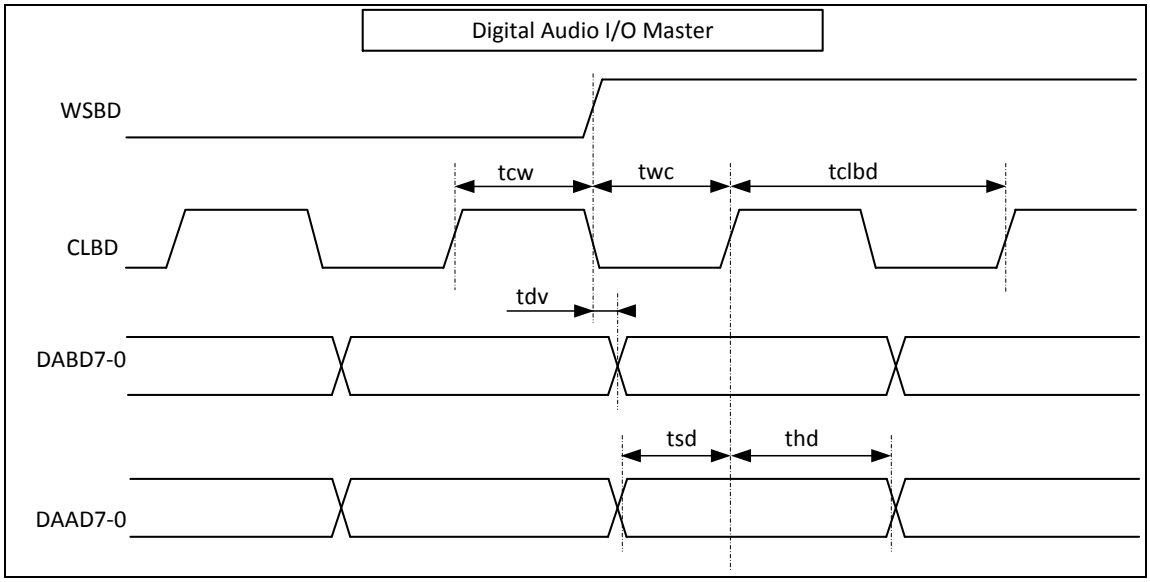
The choice of clock factors is done by the firmware. As an example, table below show some possible clock combinations with 12.288MHz Xtal.

Sampling Rate @ Xtal=12.288MHz	CKOUT freq	CKOUT/WSBD freq ratio	CLBD freq	CLBD/WSBD freq ratio
48kHz	12.288MHz	256	3.072MHz	64
48kHz	24.576MHz	512	3.072MHz	64
96kHz	12.288MHz	128	6.144MHz	64
96kHz	24.576MHz	256	6.144MHz	64
192kHz	24.576MHz	128	12.288MHz	64

Note: WSBD/CLBD ratio is always 64.

8.9.1. Timing

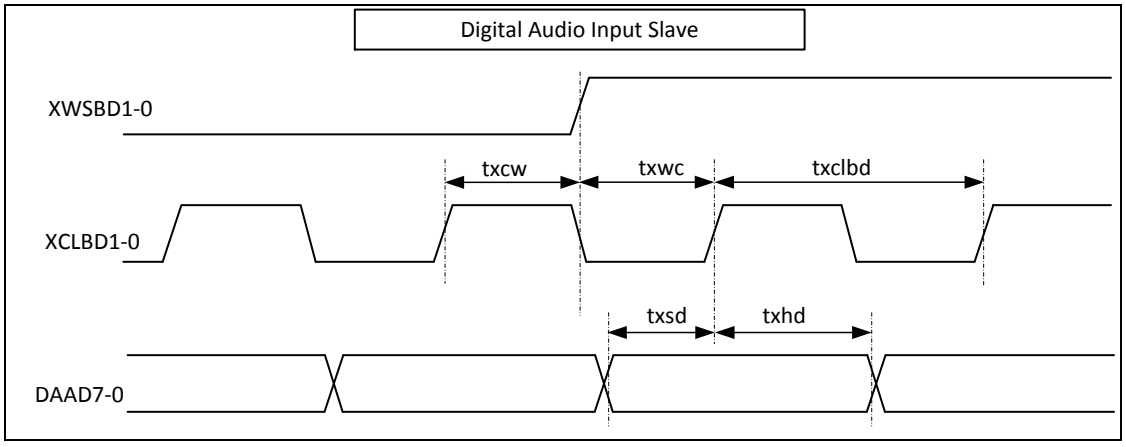
8.9.1.1. Master Mode



cpck is related to CLBD frequency: cpck = 1/(2*CLBD_freq)

Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	cpck -11	-	-	ns
WSBD change to CLBD rising	twc	cpck -11	-	-	ns
DABD valid after CLBD falling	tdv	-11	-	11	ns
DAAD valid prior CLBD rising	tsd	20	-	-	ns
DAAD valid after CLBD rising	thd	20	-	-	ns
CLBD cycle time	tclbd	-	2* cpck	-	ns

8.9.1.2. Slave Mode

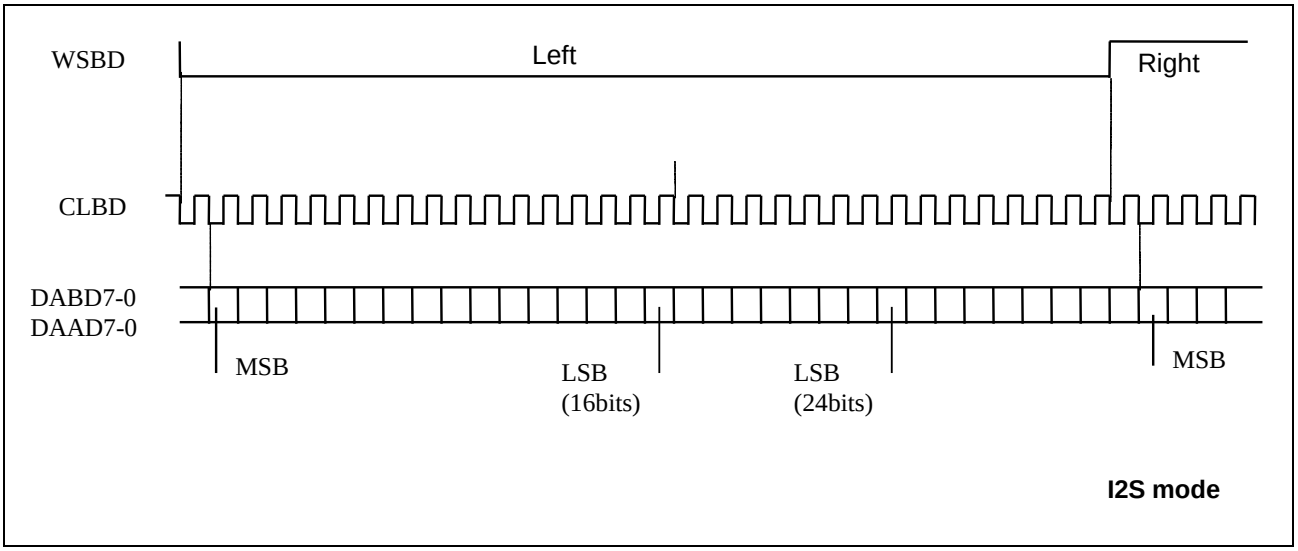


xpck is related to XCLBD frequency: xpck = 1/(2*XCLBD_freq)

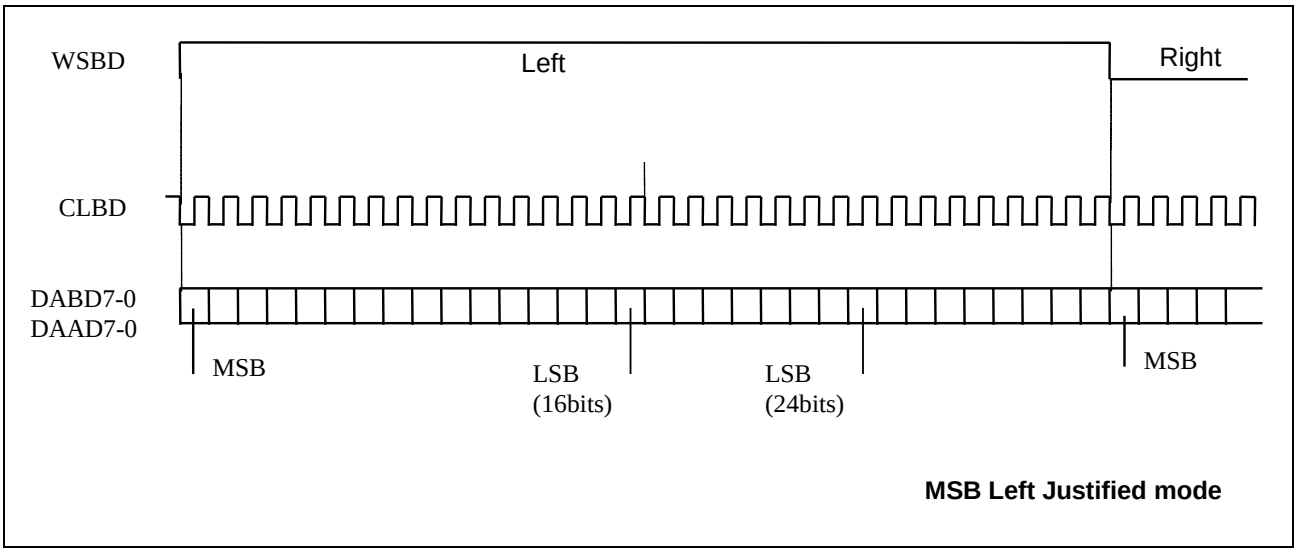
Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	txcw	20	-	-	ns
WSBD change to CLBD rising	txwc	20	-	-	ns
DAAD valid prior CLBD rising	txsd	20	-	-	ns
DAAD valid after CLBD rising	txhd	20	-	-	ns
CLBD cycle time	txclbd	-	2* xcpck	-	ns

8.9.2. Digital Audio Format

SAM5916B can generate I2S or MSB Left justified digital audio format. Master Clock CLBD can be 128xFs, 256xFs, 512xFs, 192xFs, 384xFS or 768xFs. Format and clock ratio are selected by firmware.



I2S mode



MSB Left Justified mode

8.10. SPDIF Digital audio

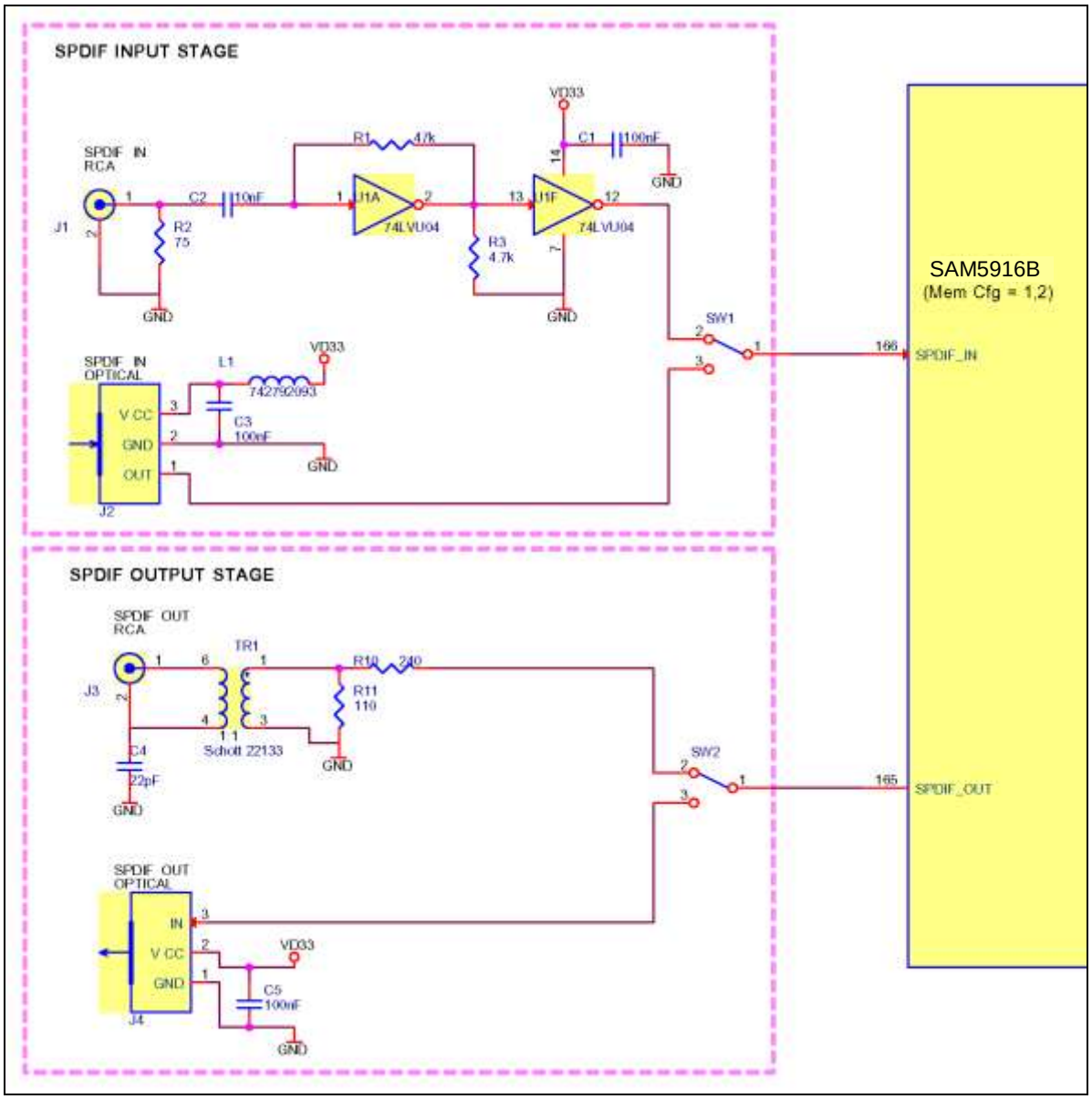
The SPDIF Digital Audio Interface Controller implements the IEC60958 interface features (commonly known as Sony/Philips Digital Interface), a unidirectional and self-clocking interface for connecting digital audio equipment using the linear PCM coded audio samples.
Receiver and Transmitter modes are supported at the same time.

Pins used:
SPDIF_IN: Serial data input
SPDIF_OUT: Serial data output

Data mode capabilities:
- Sample rate from 3kHz to 192kHz
- 24 bit per sample

8.10.1. Reference Schematic

Schematic below is example design for SPDIF IN and OUT interface with SAM5916B.



8.11. USB 2.0 Ports

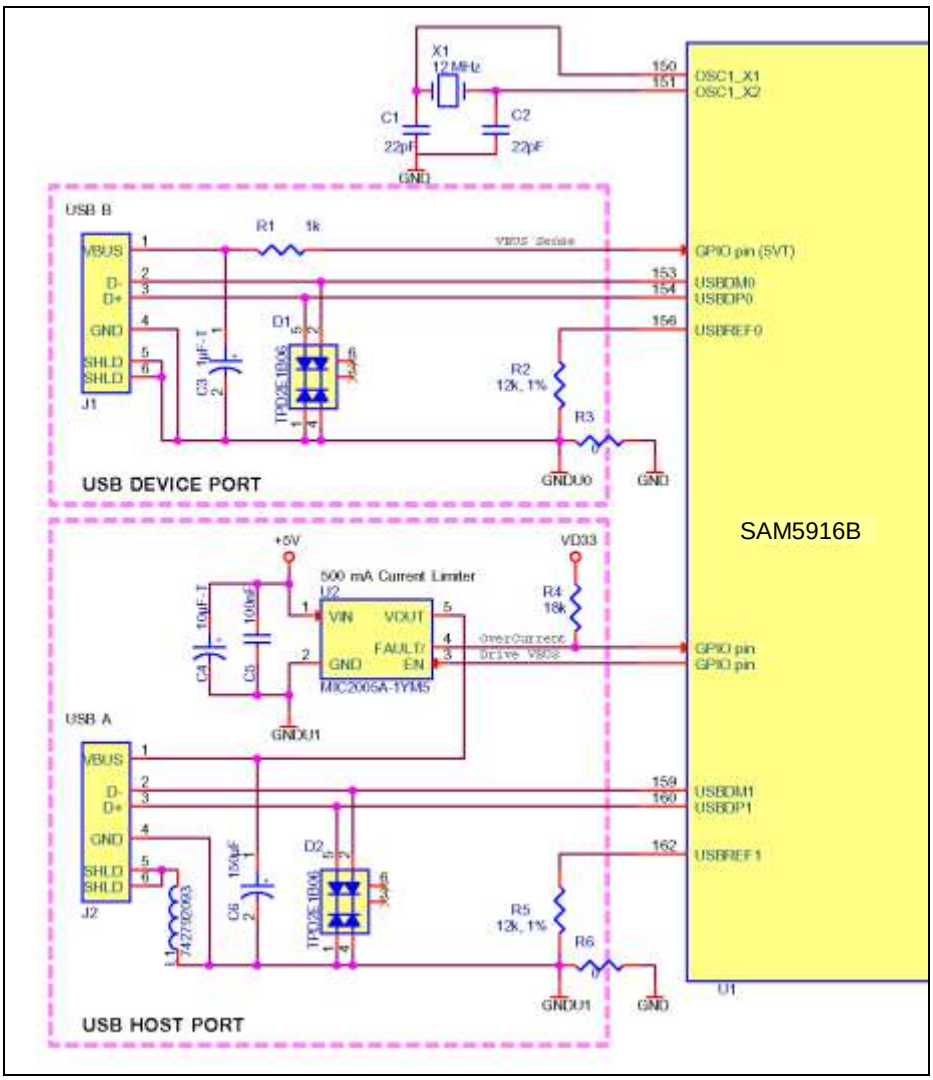
SAM5916B offer two USB 2.0 (High-Speed) ports:
- USB Port0 can be used as Device, Host or Dual Role
- USB Port1 can be used only as Host

Pins used:

OSC1_X1-OSC1_X2:	12MHz Crystal connection
USBDM0-USBDP0:	Differential analog IO for port 0
USBREF0:	Connection to 12kΩ ± 1% reference resistor for port 0
USBID:	A or B device detection for port 0 in Dual Role Mode (input)
USBDM1-USBDP1:	Differential analog IO for port 1
USBREF1:	Connection to 12kΩ ± 1% reference resistor for port 1

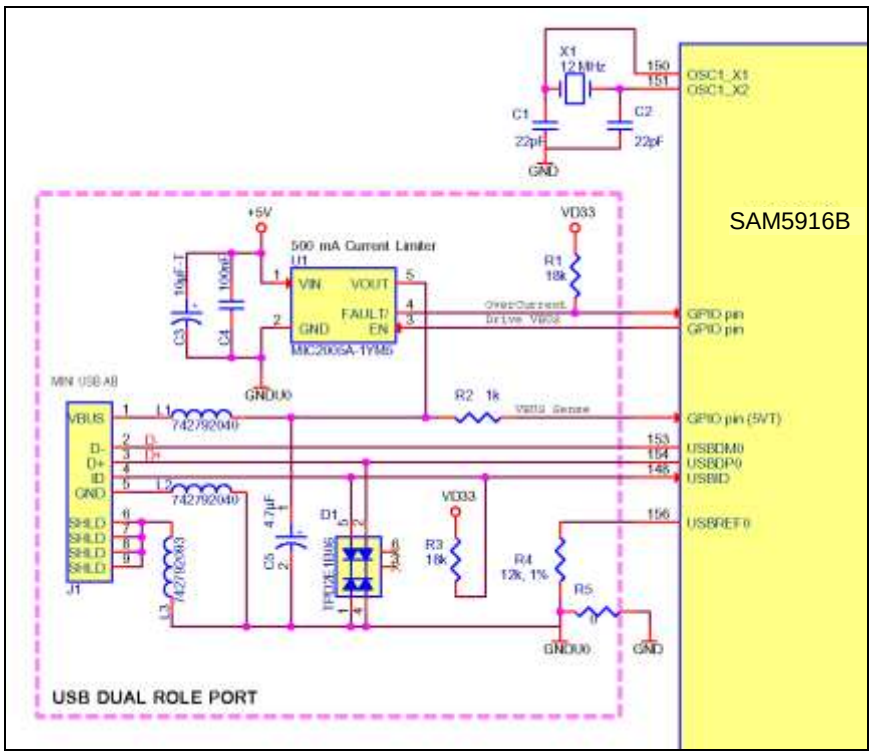
8.11.1. USB Device Port and USB Host Port

Schematic below can be used as reference for:
- application with one USB Device Port
- application with one USB Host Port
- application with one USB Device Port and one USB Host Port



8.11.2. USB Dual Role Port

Schematic below can be used as reference for application with on Dual Role Port.



8.12. Ethernet Media Access Control

8.12.1. Overview

SAM5916B can access Ethernet through its embedded MAC (Media Access Control) connected to an external Ethernet PHY (Physical transceiver).

Network interface features:
- Support 10/100 data transfer rate
- Reduced Media Independent Interface (RMII)
- MII Management unit for access to the internal PHY registers
- Internal loopback mode

Data link layer functionality:
- Meet the IEEE 802.3 CSMA/CD standard
- Full or half duplex 10/100 (operation)
- Flexible address filtering (Up to 16MAC addresses, 512-bit hash table)
- Flow Control (with automatic Pause and Un-Pause frame generation)
- Statistical Counter for station management (MIB)

Integrated DMA
- Scatter-gather (descriptor based) architecture
- Descriptor “ring” or “chain” structures
- Arbitrary data alignment for the transmit buffers

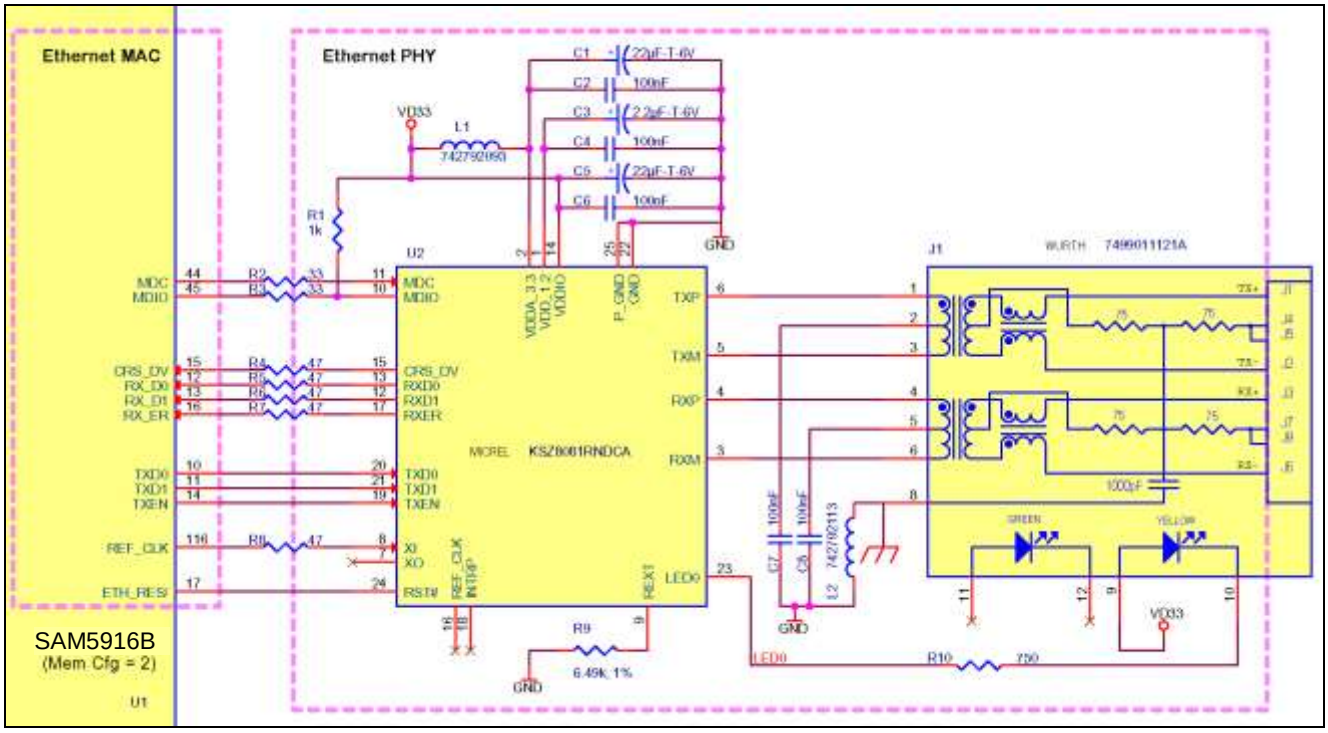
Transmit/receive dual port RAM interfaces
- Operates as internal configurable FIFOs
- Programmable transmit threshold levels
- Transmit FIFO “store and forward” functionality

Pin used:

REF_CLK:	25MHz RMII reference clock output
ETH_RES/:	Reset output
RX_ER:	RMII Receive Error input
RXD0:	RMII Receive Data 0 input
RXD1:	RMII Receive Data 1 input
CRS_DV:	RMII Carrier Sense/Receive Data Valid input
TXD0:	RMII Transmit Data 0 output
TXD1:	RMII Transmit Data 1 output
TX_EN:	RMII Transmit Enable output
MDC	MII Clock output
MDIO	MII Data I/O

8.12.2. Reference Schematic

Schematic below is example design for Ethernet interface with SAM5916B.
Ethernet PHY is made of Micrel KSZ8081 PHY device + Wurth 7499011121A LAN transformer/connector.



9. Audio Synchronization

9.1. Synchronization on external audio devices

In professional applications, it can be decided to synchronize SAM5916B audio processing on external audio flow(s) from USB, SPDIF or Ethernet interfaces. Another professional feature is synchronization on external word clock.

9.1.1. Principle

- Audio clock frequency is extracted from incoming audio flow or from external word clock and is compared with frequency currently used for internal audio processing.
- Comparison result is used to control the internal PWM generator.
- PWM generator output is filtered, and then, can drive an external VCXO.
- VCXO clock output is used as master clock for internal audio processing.

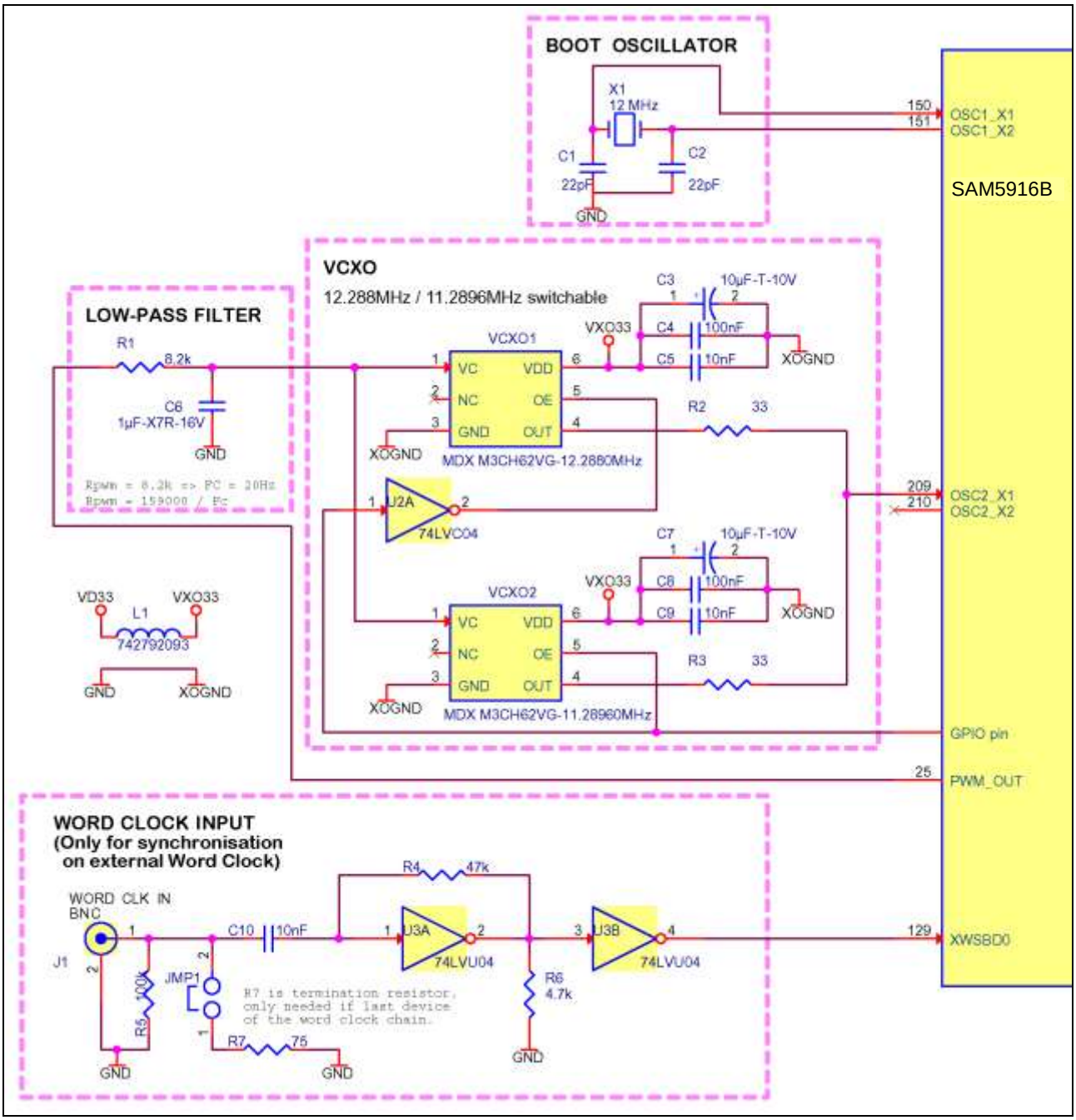
As a result, clock frequency for internal audio processing is perfectly enslaved to incoming audio flow.

Pin used:

OSC1_X1, OSC1_X2:	Connection to 12MHz crystal for USB, Ethernet and system boot.
OSC2_X1:	Clock input for audio system clock from VCXO
PWM:	PWM output
XWSBD0 (optional):	Input for external Word Clock

9.1.2. Reference schematic

Schematic below can be used as reference for synchronization on external audio flowing and optionally on external word clock.

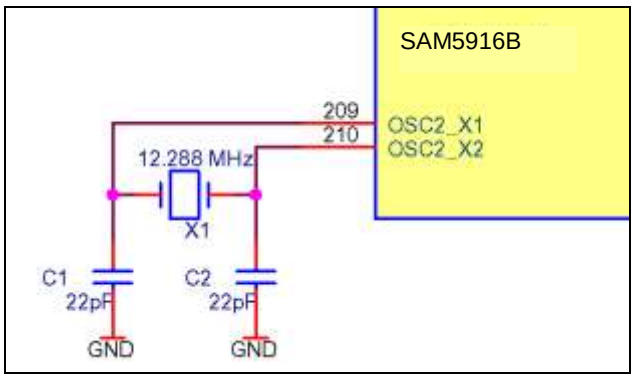


- At start-up system runs on OSC1 oscillator used as Boot oscillator.
- When environment is stabilized, firmware switches system and audio clock source from boot oscillator to second oscillator input OSC2_X1 driven by VCXO clock.

Notes:
- PCB design around VCXO is sensitive. See VCXO manufacturer relative application notes
- Crystal used on VCXO must be pullable enough to allow a sufficient frequency variation necessary to proper VCXO operation. See VCXO manufacturer relative application notes for Crystal choice.

10. Recommended Crystal Compensation

10.1. OSC2_X1 - OSC2_X2



C1 and C2 should be chosen in range 12pF-27pF. Different values lead to different oscillation characteristic and can be selected based on board layout considerations.
External feedback resistor should be avoided because there is an internal feedback resistor.

10.2. OSC1_X1 – OSC1_X2

Crystal connection on OSC1_X1 – OSC1_X2 follows the same off-chip components recommendation than crystal connection on OSC2_X1 – OSC2_X2

11. Reset and Power Down

During power-up, the RST/ input should be held low until the core is stabilized in reset state, which takes 10ms Max.
After the low to high transition of RST/, following happens:

- Oscillator OSC1 is started
- P16 program execution starts in built-in ROM
- PLL is started and stabilized after 2.5 ms typ
- P16 application program loading starts.

If RST/ is asserted low then the crystal oscillators and PLLs will be stopped.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256
- ADC can be disabled
- Controllers for USB, Ethernet or DDR/SDRAM can be individually switched off

11.1. Power-up sequence

At power-up the following sequence is executed:

1. STIN is sensed. If HIGH, then the built-in debugger is started.
2. If MC1-0 bits were preprogrammed they are read from eFuse. Otherwise MC1-0 pins are sensed and corresponding Memory Config is set
3. ROM boot tries to identify source for firmware. For that it tries to find “DR” marker for Dream firmware. This step is done in slow mode (PLL not started). During this step, rom boot set the minimum of primary functions to avoid any potential conflict of some pins. Accesses to memories are done with longest access time, most simple protocol (accessing for example Quad SPI memory in single mode rather than quad mode). ROM boot searches source in following order:
   a) Main Memory. According to Memory Config, Main Memory can be: NOR Flash or NAND Flash,
   b) Multi-Purpose Quad SPI
4. If valid firmware has not been found, firmware download from a host processor is assumed into internal RAM (56k x16 max) via Host Parallel Interface.
   a) The byte 0ACh is written to the host. The host checks status and can recognize that the chip is ready to accept program download.
   b) The host sends the Boot_Info table (low byte first, 20 * 2 bytes). Boot_Info table contains info on firmware size, primary and secondary functions setting, memory and software config. The Boot_Info table is generated by SamVS , and is located in the firmware binary file at word addresses 1-20.
   c) SAM5916B sends ACh when initializations are ready
   d) The host sends the SAM5916B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
   "DownLoadSize" is defined in the Boot_Info table at word address 3.
   e) The byte 0ACh is written to the host. The host checks status and can recognize that the chip has accepted the firmware.
   f) SAM5916B starts the firmware.

   Note: Be aware that at boot time the IRQ signal is not used, the Host CPU must read the port status register (TE/RF bits) before sending or reading a data byte to/from SAM5916B via 8-bit parallel port.

11.2. Pin status in Power-down mode

Table below shows the status of each I/O pin in Power-down mode (RST/ Low)

Pin name	Status in Power-down mode
VIN	ANA IN
RST/	IN driven Low
TEST	IN with Pull-down resistor
STIN	IN with Pull-down resistor
STOUT	IN with Pull-up resistor
CKOUT, CLBD, WSBD	IN with Keeper resistor
MIDI_IN1, MIDI_OUT1	IN with Keeper resistor
All Memory pins (MEM)	TRISTATE output
All other I/O pins	IN with Keeper resistor

Note:

- Keeper resistor can be pull-up or to pull-down resistor. This will depend on logic state at the pin where it is connected when switching to Power-down mode.
    - If logic state is ‘Low’ when entering Power-down mode, keeper resistor will be pull-down
    - If logic state is ‘High’ when entering Power-down mode, keeper resistor will be pull-up

12. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

12.1. GND, VD33, VM, VC12, VD12 distribution, decoupling

All GND, VD33, VM, VC12, VD12 pins should be connected. A GND plane is strongly recommended. The board GND, VD33, VM and VC12, VD12 distribution should be in grid form.

Recommended VD12 decoupling is 100nF+10nF at each VD12 pin of the IC with additional 10µFT on two opposite sides

VC12 requires 10µFT +100nF on each pin.

Minimum recommended VM decoupling is 0.1µF at half of VM pins. 10nF should be connected at the other half of VM pins. 10µFT should be also added on two opposite sides.

Recommended VD33 decoupling is 0.1µF at half of VD33 pins.
VD33R requires a single 10µFT decoupling.
VD330 requires a single 100nF decoupling.
VD33U0 and VD33U1 require 10µFT+100nF+10nF capacitors on each.

12.2. Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

12.3. Busses

Parallel layout from D15-D0 and WA27-WA0/WD15-WD0 should be avoided. The D15-D0 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA27-WA0/WD15-WD0 which can corrupt address and/or data on these busses.
Parallel layout from D15-D0 and MA18-MA0/MD15-MD0 should be avoided.
Parallel layout from D15-D0 and DRA13-DRA0/DRBA1-DRBA0/DRDQ15-DRDQ0/DRDS1-DRDS0 should be avoided.

A ground plane should be implemented below the D16-D0 bus, which connects both to the host and to the SAM5916B GND.

A ground plane should be implemented below the WA27-WA0/WD15-WD0 bus, which connects both to the NOR Flash grounds and to SAM5916B.

A ground plane should be implemented below the MA18-MA0/MD15-MD0 bus, which connects both to the SRAM grounds and to SAM5916B

A ground plane should be implemented below the NDIO15-NDIO0 bus, which connects both to the NAND Flash grounds and to SAM5916B.

12.4. DDR SDRAM and SDR SDRAM

For SDRAM following layout rules should be applied:

- 6 layer PCB is needed for DDR SDRAM. Layer 1 = Signal + Ground plane, Layer 2 = Ground plane, Layer 3 = Signal, Layer 4 = Signal, Layer 5 = Power Supply Plane, Layer 6 = Signal + Ground plane.
- 4 layer PCB is needed for SDR SDRAM. Layer 1 = Signal + Ground plane, Layer 2 = Ground plane, Layer 3 = Signal + Power Supply Plane, Layer 4 = Signal + Ground plane

- If 4 DDR memory devices, it is recommended to implement 2 devices on each side of the PCB.

- All DRDQ15-DRDQ0, DRDS0-DRDS1, DRDM0-DRDM1 should be routed together and should have same length, considering all the SDRAM devices. It means that each DRDQx signal should have the same length from its SAM5916B DRDQx pin to each of the DRDQx pin of each SDRAM device. It also means that all the DRDQx and DRDMx signals should have the same length. In case of DDR SDRAM, this length should be also the one for DRDSx signals. Tolerance should be lower than ±.5mm.

- All DRDA13-DRDA0, DRDBA1-DRDBA0 should be routed together and should have the same length, considering one SDRAM device. It means that all the DRDAx/DRDBAx signals should have a same length L1 from SAM5916B to the first DDR device and a same length L2 from SAM5916B to the second DDR device,.... Tolerance should be lower than +/-2mm.

- DRRAS/, DRCAS/, DRWE/, DRCKE should be routed together and should have the same length.

- SDRAM systems have only a single-ended clock (DRCK), so the important trace-matching relationship is not to a second differential clock trace but instead to the other groups. Match clock traces to data group traces within ±12mm. If multiple clocks are transmitted from the controller to components, all clock-pair traces should be equivalent to within ±0.5mm. Matching trace lengths to this level of accuracy helps minimize skew.
  For both DDR and SDRAM, also match clock traces to each signal trace in the address and command groups to within ±10mm. If clock traces cannot be matched to the trace lengths of these groups within 10mm, then all clock trace lengths must be increased as a group. The longest-to-shortest trace-length difference must be ≤20mm, so both longest and shortest traces determine how much length must be added to all clock lines.

- If DDR SDRAM, VREF must be equal to VM/2, generated with a resistive divider. Both resistors must have the same value (1% precision). Suggested range is 50-150 Ω. Proper decoupling at VREF source, VREF pin of DDR device and VREF pin of SAM5916B is recommended.

12.5. ESD and EMI

Below are some tips that allow reaching good protective level again EMI and ESD with SAM5916B. This list is no exhaustive.

- Equipotentiality of the ground plane is a major point to avoid weakness against EMI. The 4 layer design is the best solution. When 2 layer design, the unused zones of the component side should be filled with ground planes connected with a lot of through holes to the ground plane of the solder side.

- High speed clock and signals trace should be short and shielded. Serial resistor or RC filter can be added close to the source to filter harmonics.

- Main power supply, before regulators should be protected with T filter like Murata NFM41PC204F1H3 and serial choke coil like LQH43CN220K03

- Connectors should be protected. EMI filters like Murata NFM21CC102R1H3 should be implemented on the clock and data lines, close to their connection on the connectors. Power supply lines can be protected with Murata BLM21RK102SN1 or Wurth 742792093.

- Each power supply pin of SAM5916B and of all active components should be decoupled with 100nF X7R capacitor and 470pF NPO or COG capacitor. A 10µF capacitor should be added close to the SAM5916B Xtal.

- Each active component should be isolated from the main power supply with a serial inductor on its power supply lines. Murata BLM21RK102SN1 or Wurth 742792093 can be used for this.

- Address, Data, Chip select, Reset signals for SAM5916B can be isolated from their environment with serial 33 Ohm resistor close to SAM5916B.

- Data, clock lines signals for DAC should be isolated from their environment with serial 22 Ohm resistors close to the DAC.

- On sensitive lines like Reset, 470pF NPO or COG capacitor can be added, close to SAM5916B.

13. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (WinXP and up). Within the environment, it is possible to:

- Edit
- Assemble / Compile (C Compiler for P16XT included) and build firmware binary file
- Debug on real target (In Circuit Emulation)
- Program external NOR Flash, NAND Flash, serial Flash/EEPROM on target.

Separated tools allowing programming the internal eFuses of SAM5704B, e.g. “ProgSam” provided by Dream for in-circuit programming of eFuses and Firmware/sound bank.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using serial communication at 57.6 kbauds. Dream provides a USB debug interface (5000DBG-IF) for easy use.

A library of frequently used functions is available within the SamVS-C development package (5916PIA-C-PDK). Thus time to market is optimized by testing directly on the final prototype.

Dream engineers are available to study customer specific applications.

14. Die Revision

All features are same in all die revisions, excepted what is described in the table below.

Die Revision	Package Marking	Notes
A	SAM5916	AES sound bank encryption mode cannot be used
B	SAM5916B	AES sound bank encryption mode can be used but only in condition: Memory Clock = System Clock/2.

Dream Contact

info@dream.fr

Website

http://www.dream.fr